MOS
LSI

TMS 4045 JL, NL; TMS 4047 JL, NL
1024 WORD BY 4-BIT STATIC RAM

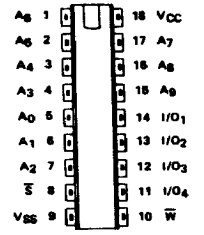
NOVEMBER 1977

- 1024 X 4 Organization
- Single +5 V, ±10% Supply
- High Density 18-and 20-pin Packages
- Fully Static Operation (No clocks, no refresh, no timing strobe)
- 5 Performance Ranges

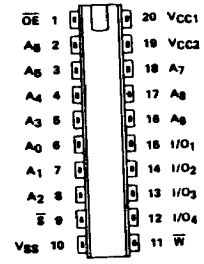
	ACCESS TIME (MAX)	READ OR WRITE CYCLE TIME (MIN)
TMS 4045-15, TMS 4047-15	150 ns	150 ns
TMS 4045-20, TMS 4047-20	200 ns	200 ns
TMS 4045-25, TMS 4047-25	250 ns	250 ns
TMS 4045-30, TMS 4045-30	300 ns	300 ns
TMS 4045-45, TMS 4047-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity With Standard TTL Loads — No Pull-Up Resistors Required
- Common I/O With Three-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 1 Series 74 or 74S TTL Load — No Pull-Up Resistors Required
- Low Power Dissipation
  - 400 mW (–25, –30, –45) Maximum
  - 550 mW (–15, –20) Maximum

TMS 4045
18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4047
20-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



PIN NAMES	
A_0-A_9	Addresses
I/O_1-I/O_4	Data input/output
$\overline{OE}$	Output Enable
$\overline{S}$	Chip Select
V_{CC} (TMS 4045)	+5 V Supply
V_{CC1} (TMS 4047)	+5 V Supply (array only)
V_{CC2} (TMS 4047)	+5 V Supply (periphery only)
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 1024 words of 4 bits. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74 or 74S TTL. No pull-up resistors are required. The TMS 4045/4047 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Both the TMS 4045 and TMS 4047 are characterized to retain data at V_{CC} = 2.4 V to reduce power dissipation. Furthermore for applications such as battery backup, the TMS 4047 has separate V_{CC} pin for the array and periphery, and data will be retained if power solely to the array is maintained.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222