

SN54LS183, SN74LS183 DUAL CARRY-SAVE FULL ADDERS

SDLS137

BULLETIN NO. DL-57711848, OCTOBER 1976—REVISED MARCH 1988

- For Use in High-Speed Wallace-Tree Summing Networks
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design

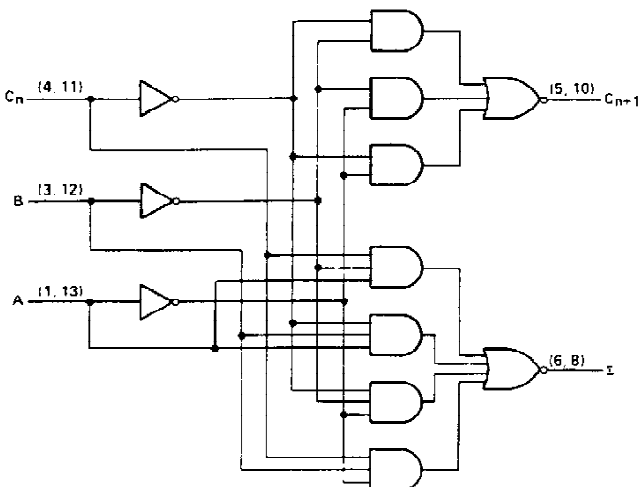
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TYPES	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'LS183	15 ns	23 mW per bit

description

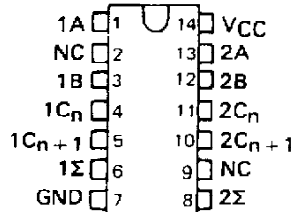
These dual full adders feature an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two gate delays. The circuits utilize high-speed, high-fan-out, transistor-transistor logic (TTL), but are compatible with both DTL and TTL families. SN54LS183 is characterized for operation over the full military temperature range of -55°C to 125°C ; SN74LS183 is characterized for operation from 0°C to 70°C .

logic diagram (each adder)

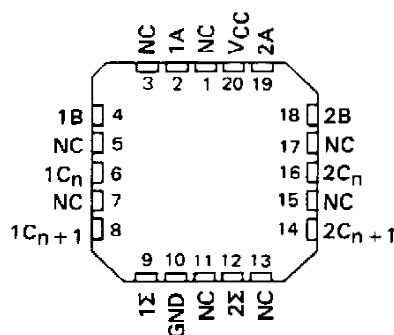


Pin numbers shown are for D, J, N, and W packages.

SN54LS183 . . . J OR W PACKAGE
SN74LS183 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS183 . . . FK PACKAGE
(TOP VIEW)



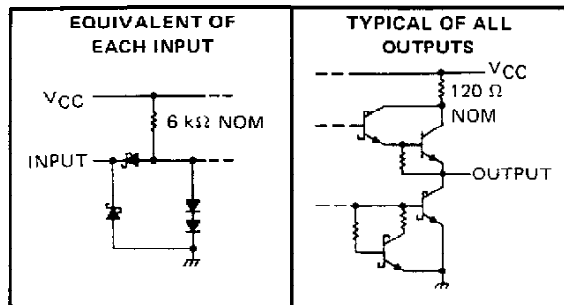
NC - No internal connection

FUNCTION TABLE
(EACH ADDER)

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

H = high level, L = low level

schematics of inputs and outputs



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TEXAS
INSTRUMENTS

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SN54LS183, SN74LS183 DUAL CARRY-SAVE FULL ADDERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS183 Circuits	-55°C to 125°C
SN74LS183 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

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NOTE 1: Voltage values, except interemitter voltage, are with respect to network ground terminal.

recommended operating conditions

	SN54LS183			SN74LS183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	-400			-400			μ A
Low-level output current, I_{OL}	4			8			mA
Operating free-air temperature, T_A	-55			0			70 °C

electrical characteristics over recommended operation free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS183			SN74LS183			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IH} High-level input voltage		2			2			V	
V_{IL} Low-level input voltage		0.7			0.8			V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$	0.25		0.4	0.25		0.4	V	
	$I_{OL} = 8 \text{ mA}$				0.35		0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.3			0.3			mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	60			60			μ A	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-1.2			-1.2			mA	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA	
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX},$ See Note 3	10			17	10		17	mA
I_{CCH} Supply current, all outputs high	$V_{CC} = \text{MAX},$ See Note 4	8			14	8		14	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. I_{CCL} is measured with all outputs open and all inputs grounded.

4. I_{CCH} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$	9		15	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 5	20		33	ns

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



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