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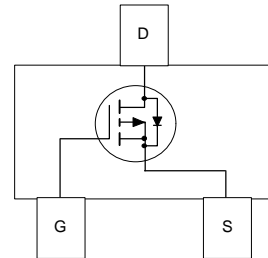
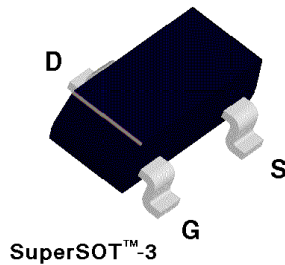
## NDS356AP P-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

SuperSOT™-3 P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- -1.1 A, -30 V,  $R_{DS(ON)} = 0.3 \Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 0.2 \Omega @ V_{GS} = -10 \text{ V}$ .
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol         | Parameter                                    | NDS356AP   | Units            |
|----------------|--|------------|------------------|
| $V_{DSS}$      | Drain-Source Voltage                         | -30        | V                |
| $V_{GSS}$      | Gate-Source Voltage - Continuous             | $\pm 20$   | V                |
| $I_D$          | Maximum Drain Current - Continuous (Note 1a) | $\pm 1.1$  | A                |
|                | - Pulsed                                     | $\pm 10$   |                  |
| $P_D$          | Maximum Power Dissipation (Note 1a)          | 0.5        | W                |
|                | (Note 1b)                                    | 0.46       |                  |
| $T_J, T_{STG}$ | Operating and Storage Temperature Range      | -55 to 150 | $^\circ\text{C}$ |

### THERMAL CHARACTERISTICS

|                 |   |     |                           |
|-----------------|---|-----|---------------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 250 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1)     | 75  | $^\circ\text{C}/\text{W}$ |

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Symbol                                    | Parameter                         | Conditions   | Min                       | Typ  | Max  | Units         |               |
|---|-----------------------------------|--|---------------------------|--|------|---------------|---------------|
| <b>OFF CHARACTERISTICS</b>                |                                   |  |                           |  |      |               |               |
| $BV_{DSS}$                                | Drain-Source Breakdown Voltage    | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$   | -30                       |  |      | V             |               |
| $I_{DSS}$                                 | Zero Gate Voltage Drain Current   | $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$   |                           |  | -1   | $\mu\text{A}$ |               |
|   |                                   |  | $T_J = 55^\circ\text{C}$  |  |      | -10           | $\mu\text{A}$ |
| $I_{GSSF}$                                | Gate - Body Leakage, Forward      | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$  |                           |  | 100  | nA            |               |
| $I_{GSSR}$                                | Gate - Body Leakage, Reverse      | $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$   |                           |  | -100 | nA            |               |
| <b>ON CHARACTERISTICS</b> (Note 2)        |                                   |  |                           |  |      |               |               |
| $V_{GS(th)}$                              | Gate Threshold Voltage            | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$   | -0.8                      | -1.6   | -2.5 | V             |               |
|   |                                   |  | $T_J = 125^\circ\text{C}$ | -0.5   | -1.3 |               | -2.2          |
| $R_{DS(on)}$                              | Static Drain-Source On-Resistance | $V_{GS} = -4.5\text{ V}, I_D = -1.1\text{ A}$  |                           | 0.25   | 0.3  | $\Omega$      |               |
|   |                                   |  | $T_J = 125^\circ\text{C}$ |  | 0.35 |               | 0.4           |
|   |                                   |  |                           | $V_{GS} = -10\text{ V}, I_D = -1.3\text{ A}$ |      |               | 0.14          |
| $I_{D(on)}$                               | On-State Drain Current            | $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$   | -3                        |  |      | A             |               |
| $g_{FS}$                                  | Forward Transconductance          | $V_{DS} = -5\text{ V}, I_D = -1.1\text{ A}$  |                           | 2  |      | S             |               |
| <b>DYNAMIC CHARACTERISTICS</b>            |                                   |  |                           |  |      |               |               |
| $C_{iss}$                                 | Input Capacitance                 | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1.0\text{ MHz}$                        |                           | 280  |      | pF            |               |
| $C_{oss}$                                 | Output Capacitance                |  |                           | 170  |      | pF            |               |
| $C_{rss}$                                 | Reverse Transfer Capacitance      |  |                           | 65   |      | pF            |               |
| <b>SWITCHING CHARACTERISTICS</b> (Note 2) |                                   |  |                           |  |      |               |               |
| $t_{D(on)}$                               | Turn - On Delay Time              | $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$<br>$V_{GS} = -10\text{ V}, R_{GEN} = 50\ \Omega$ |                           | 8  | 15   | ns            |               |
| $t_r$                                     | Turn - On Rise Time               |  |                           | 17   | 30   | ns            |               |
| $t_{D(off)}$                              | Turn - Off Delay Time             |  |                           | 53   | 90   | ns            |               |
| $t_f$                                     | Turn - Off Fall Time              |  |                           | 38   | 80   | ns            |               |
| $Q_g$                                     | Total Gate Charge                 | $V_{DS} = -10\text{ V}, I_D = -1.1\text{ A},$<br>$V_{GS} = -5\text{ V}$                      |                           | 3.4  | 4.4  | nC            |               |
| $Q_{gs}$                                  | Gate-Source Charge                |  |                           | 0.7  |      | nC            |               |
| $Q_{gd}$                                  | Gate-Drain Charge                 |  |                           | 1.5  |      | nC            |               |

### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol  | Parameter   | Conditions                                     | Min | Typ  | Max   | Units |
|---|---|--|-----|------|-------|-------|
| <b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b> |   |  |     |      |       |       |
| $I_S$   | Maximum Continuous Source Current                 |  |     |      | -0.42 | A     |
| $I_{SM}$  | Maximum Pulsed Drain-Source Diode Forward Current |  |     |      | -10   | A     |
| $V_{SD}$  | Drain-Source Diode Forward Voltage                | $V_{GS} = 0\text{ V}$ , $I_S = -0.42$ (Note 2) |     | -0.8 | -1.2  | V     |

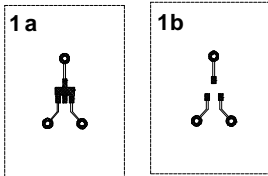
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical  $R_{\theta JA}$  using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 250°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- 270°C/W when mounted on a 0.001 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

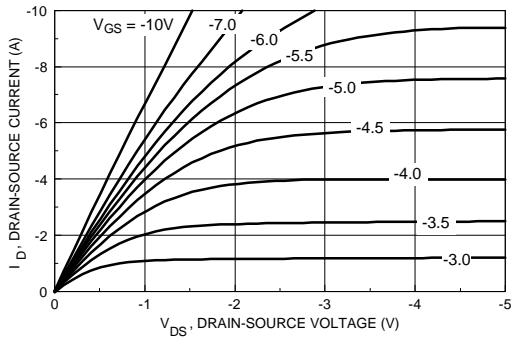


Figure 1. On-Region Characteristics.

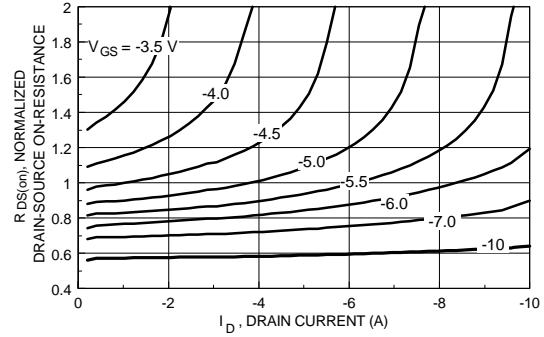


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

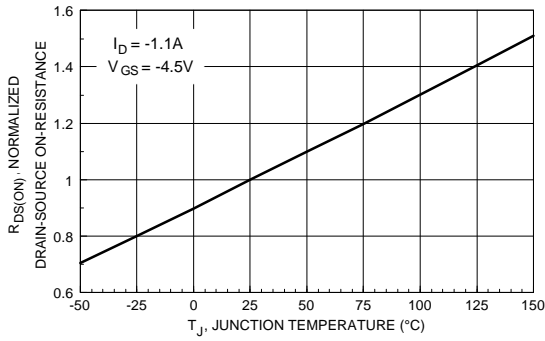


Figure 3. On-Resistance Variation with Temperature.

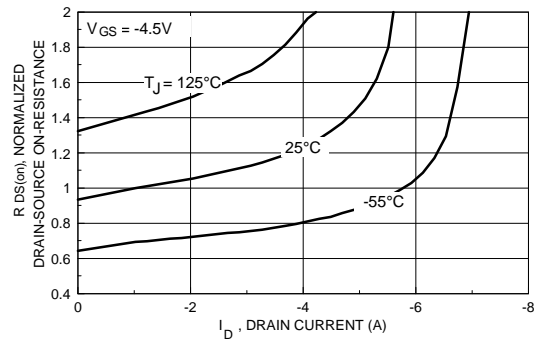


Figure 4. On-Resistance Variation with Drain Current and Temperature.

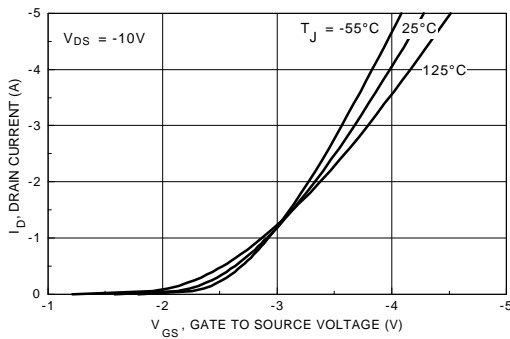


Figure 5. Transfer Characteristics.

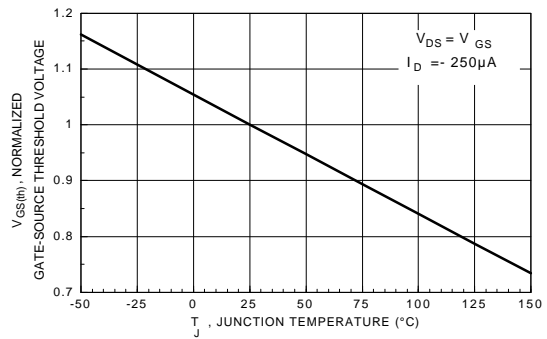
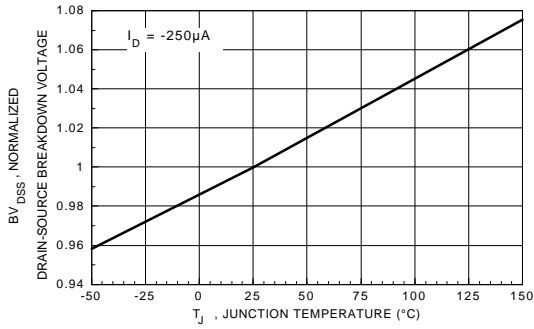
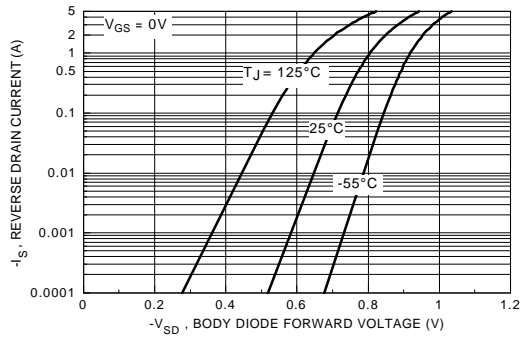


Figure 6. Gate Threshold Variation with Temperature.

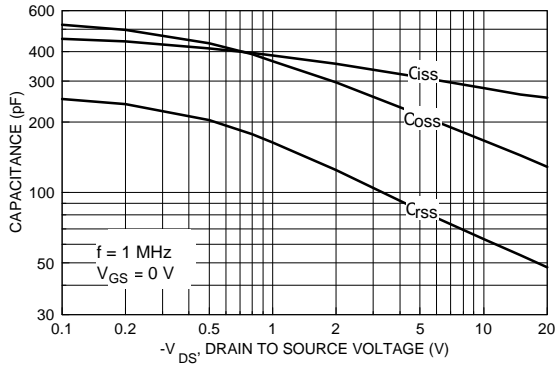
## Typical Electrical Characteristics (continued)



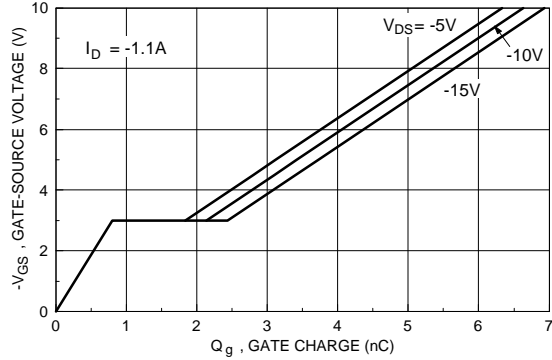
**Figure 7. Breakdown Voltage Variation with Temperature.**



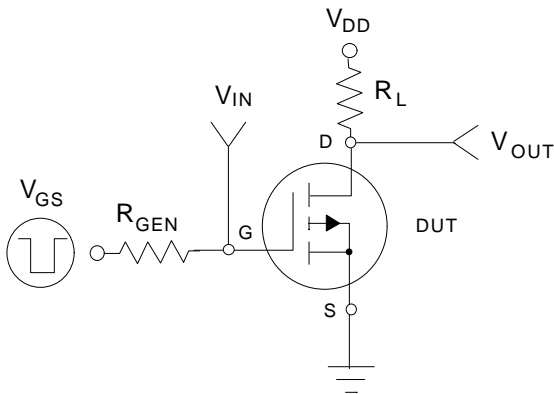
**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.**



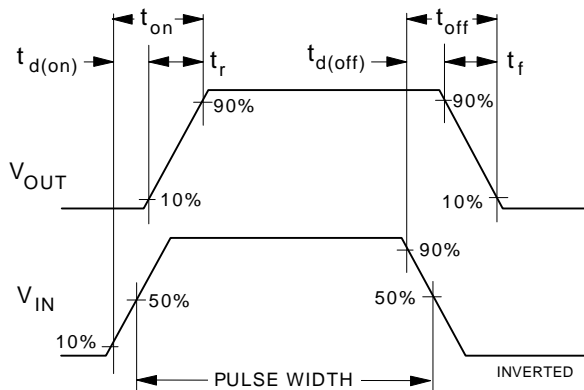
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**

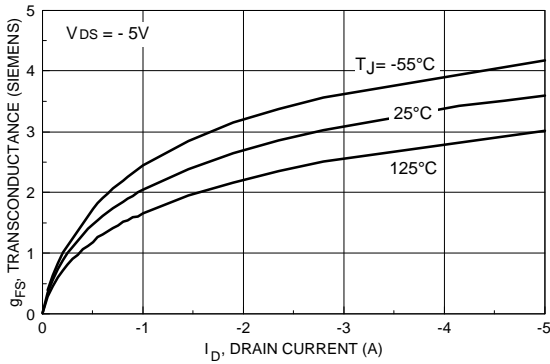


**Figure 11. Switching Test Circuit.**

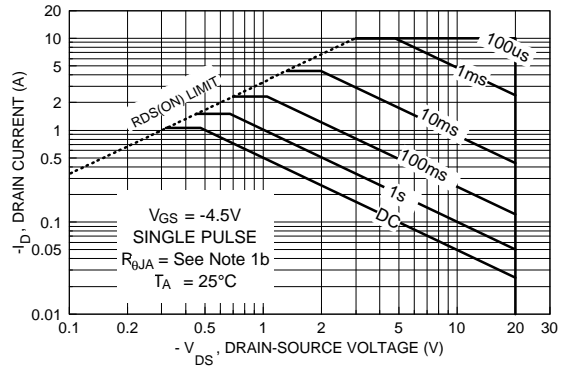


**Figure 12. Switching Waveforms.**

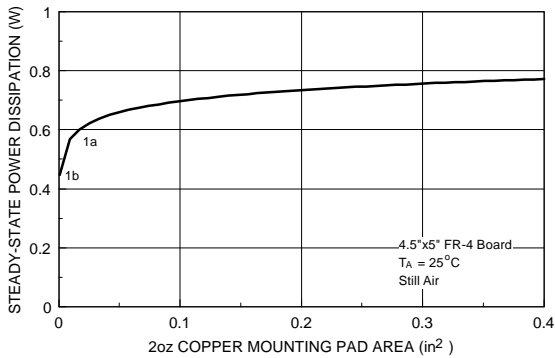
**Typical Electrical Characteristics (continued)**



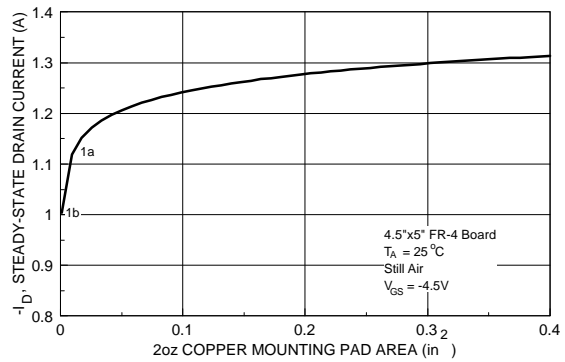
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



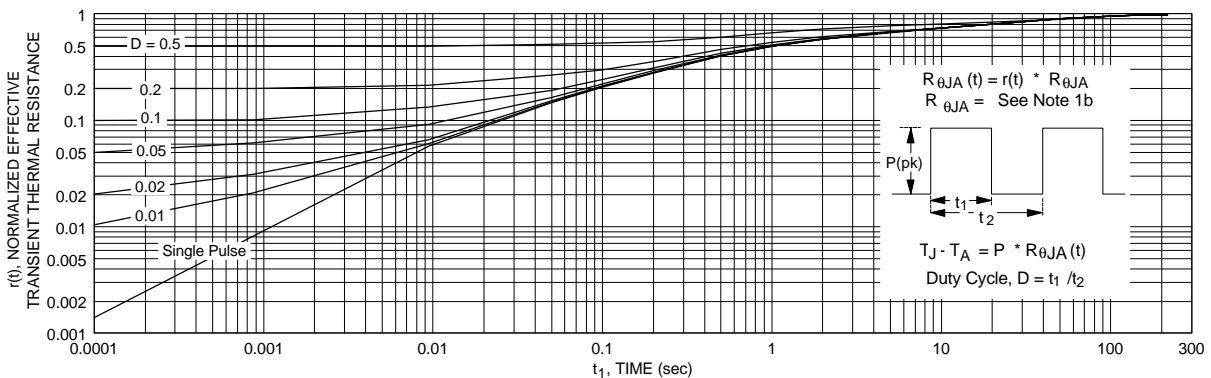
**Figure 14. Maximum Safe Operating Area.**



**Figure 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 17. Transient Thermal Response Curve.**

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

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