74HC4052; 74HCT4052

Dual 4-channel analog multiplexer/demultiplexer

Product data sheet

1. General description

The 74HC4052; 74HCT4052 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4052B. The device is specified in compliance with JEDEC standard no. 7A.

The 74HC4052; 74HCT4052 is a dual 4-channel analog multiplexer/demultiplexer with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin $\overline{E}$). When pin $\overline{E}$ = LOW, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin $\overline{E}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (pins S0, S1 and $\overline{E}$). The V_{CC} to GND ranges are 2.0 V to 10.0 V for the 74HC4052 and 4.5 V to 5.5 V for the 74HCT4052. The analog inputs/outputs (pins nY0 to nY3 and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features

- Wide analog input voltage range from –5 V to +5 V
- Low ON resistance:
  - 80 Ω (typical) at $V_{CC} - V_{EE}$ = 4.5 V
  - 70 Ω (typical) at $V_{CC} - V_{EE}$ = 6.0 V
  - 60 Ω (typical) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built-in
- Complies with JEDEC standard no. 7A
- ElectroStatic Discharge (ESD) protection:
  - Human Body Model (HBM) EIA/JESD22-A114E exceeds 2000 V
  - Machine Model (MM) EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

founded by Philips

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4052				
74HC4052D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4052DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4052N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC4052PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4052BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4052				
74HCT4052D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4052DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4052N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT4052BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

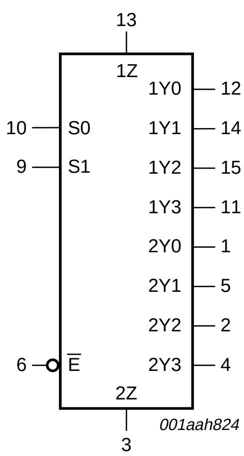


Fig 1. Logic symbol

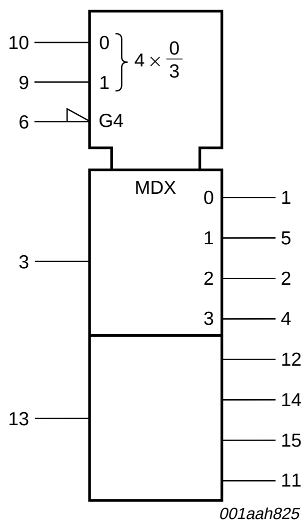


Fig 2. IEC logic symbol

7. Functional description

7.1 Function table

Table 3. Function table[1]

Input			Channel on
$\overline{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to V_{EE} = GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	–0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V		-	±20	mA
I_{SW}	switch current	-0.5 V $< V_{SW} < V_{CC} + 0.5$ V		-	±25	mA
I_{EE}	supply current			-	±20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW
P	power dissipation	per switch		-	100	mW

[1] To avoid drawing V_{CC} current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no V_{CC} current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4052			74HCT4052			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Figure 7 and Figure 8							
		V_{CC} – GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V_{CC} – V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	1.67	625	-	1.67	139	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	1.67	83	-	1.67	139	ns/V
		V_{CC} = 10.0 V	-	1.67	31	-	1.67	139	ns/V

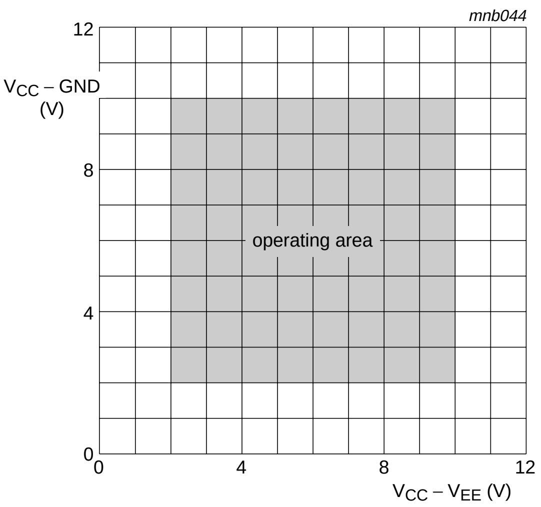


Fig 7. Guaranteed operating area as a function of the supply voltages for 74HC4052

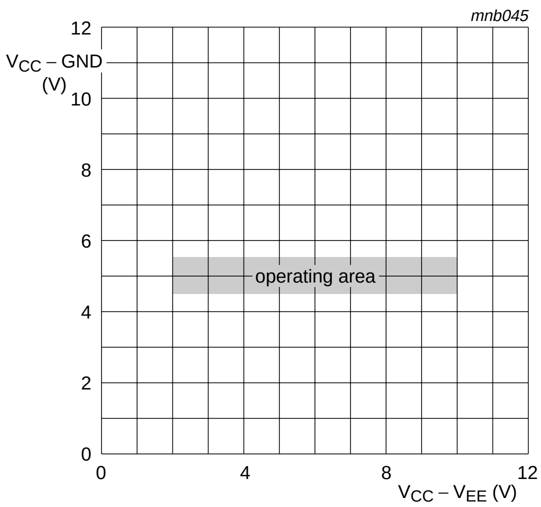


Fig 8. Guaranteed operating area as a function of the supply voltages for 74HCT4052

10. Static characteristics

Table 6. R_{ON} resistance per switch for 74HC4052 and 74HCT4052

$V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 9.
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.
For 74HC4052: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4052: V_{CC} – GND = 4.5 V and 5.5 V, V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C[1]							
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	100	225	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	90	200	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	70	165	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	80	175	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	70	150	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	60	130	Ω
		$V_{is} = V_{CC}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA		-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	90	200	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	80	175	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	65	150	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	9	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	8	-	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	6	-	Ω
T_{amb} = –40 °C to +125 °C							
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	-	195	Ω

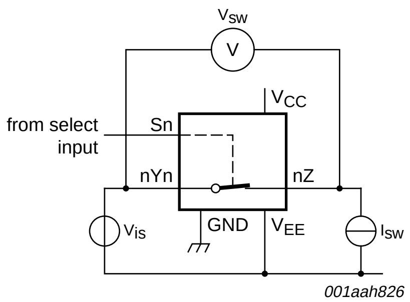
Table 6. R_{ON} resistance per switch for 74HC4052 and 74HCT4052 *...continued*

$V_I = V_{IH}$ or V_{IL}; for test circuit see Figure 9.
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.
For 74HC4052: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4052: V_{CC} – GND = 4.5 V and 5.5 V, V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	210	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	180	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	-	160	Ω
		$V_{is} = V_{CC}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_{SW} = 1000 μA		-	-	180	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

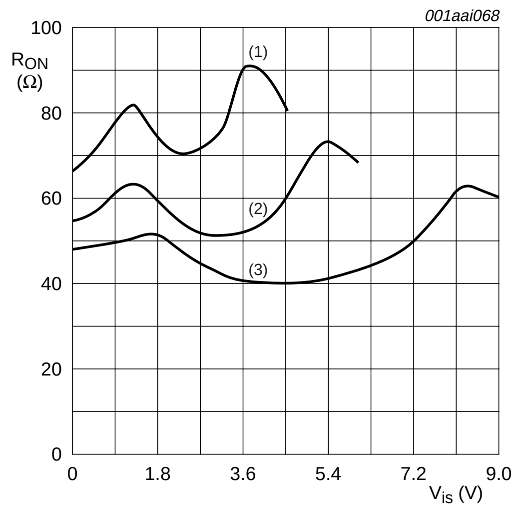
[2] When supply voltages (V_{CC} – V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



V_{is} = 0 V to (V_{CC} – V_{EE}).

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

Fig 9. Test circuit for measuring R_{ON}



V_{is} = 0 V to (V_{CC} – V_{EE}).

(1) V_{CC} = 4.5 V

(2) V_{CC} = 6 V

(3) V_{CC} = 9 V

Fig 10. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics for 74HC4052 *...continued*
Voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.
V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} − V_{EE}; see Figure 11				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} − V_{EE}; V_{CC} = 10.0 V; V_{EE} = 0 V; see Figure 12	-	-	±2.0	μA
I_{CC}	supply current	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V	-	-	160.0	μA
		V_{CC} = 10.0 V	-	-	320.0	μA

[1] All typical values are measured at T_{amb} = 25 °C.

Table 8. Static characteristics for 74HCT4052
Voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.
V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

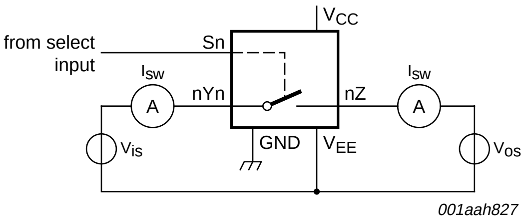
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C[1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} − V_{EE}; see Figure 11				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} − V_{EE}; see Figure 12	-	-	±2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	80.0	μA
		V_{CC} = 5.0 V; V_{EE} = −5.0 V	-	-	160.0	μA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	45	202.5	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance	independent pins Y	-	5	-	pF
		common pins Z	-	12	-	pF
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA

Table 8. Static characteristics for 74HCT4052 *…continued*

Voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.
V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

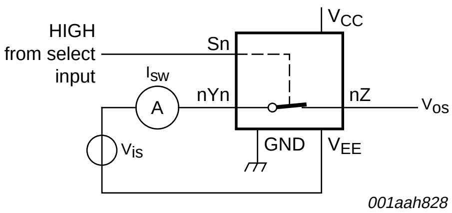
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; $V_I = V_{IH}$ or V_{IL}; $\lvert V_{SW} \rvert = V_{CC} - V_{EE}$; see Figure 11				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; $V_I = V_{IH}$ or V_{IL}; $\lvert V_{SW} \rvert = V_{CC} - V_{EE}$; see Figure 12	-	-	±2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	160.0	μA
		V_{CC} = 5.0 V; V_{EE} = –5.0 V	-	-	320.0	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	-	220.5	μA

[1] All typical values are measured at T_{amb} = 25 °C.



$V_{is} = V_{CC}$ and $V_{os} = V_{EE}$.
$V_{is} = V_{EE}$ and $V_{os} = V_{CC}$.

Fig 11. Test circuit for measuring OFF-state current



$V_{is} = V_{CC}$ and V_{os} = open-circuit.
$V_{is} = V_{EE}$ and V_{os} = open-circuit.

Fig 12. Test circuit for measuring ON-state current

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

N = number of inputs switching;

$\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics for 74HCT4052

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; for test circuit see Figure 15.
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C[1]							
t_{pd}	propagation delay	V_{is} to V_{os}; $R_L = \infty$ Ω; see Figure 13	[2]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	5	15	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	4	10	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Figure 14	[3]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	41	88	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	28	60	ns
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Figure 14	[4]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	26	63	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	21	48	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC} − 1.5 V	[5]	-	57	-	pF
T_{amb} = −40 °C to +125 °C							
t_{pd}	propagation delay	V_{is} to V_{os}; $R_L = \infty$ Ω; see Figure 13	[2]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	18	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	-	12	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Figure 14	[3]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	105	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	-	72	ns
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Figure 14	[4]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	75	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V		-	-	57	ns

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{on} is the same as t_{PZH} and t_{PZL}.

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

N = number of inputs switching;

12. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF.
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.
V_{os} is the output voltage at pins nYn or nZ, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	f_i = 1 kHz; R_L = 10 kΩ; see Figure 16					
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = –2.25 V		-	0.04	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Figure 16					
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = –2.25 V		-	0.12	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	0.06	-	%
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Figure 17					
		V_{CC} = 2.25 V; V_{EE} = –2.25 V	[1]	-	–50	-	dB
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	[1]	-	–50	-	dB
Xtalk	crosstalk	between two switches/multiplexers; R_L = 600 Ω; f_i = 1 MHz; see Figure 18					
		V_{CC} = 2.25 V; V_{EE} = –2.25 V	[1]	-	–60	-	dB
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	[1]	-	–60	-	dB
V_{ct}	crosstalk voltage	peak-to-peak value; between control and any switch; R_L = 600 Ω; f_i = 1 MHz; $\overline{E}$ or Sn square wave between V_{CC} and GND; t_r = t_f = 6 ns; see Figure 19					
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	110	-	mV
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	220	-	mV
$f_{(-3dB)}$	–3 dB frequency response	R_L = 50 Ω; see Figure 20					
		V_{CC} = 2.25 V; V_{EE} = –2.25 V	[2]	-	170	-	MHz
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	[2]	-	180	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

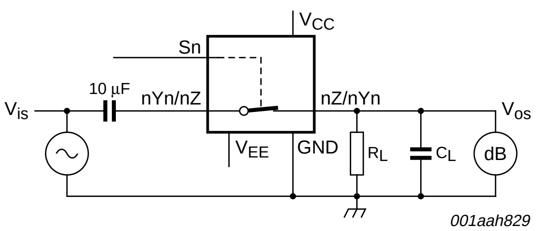
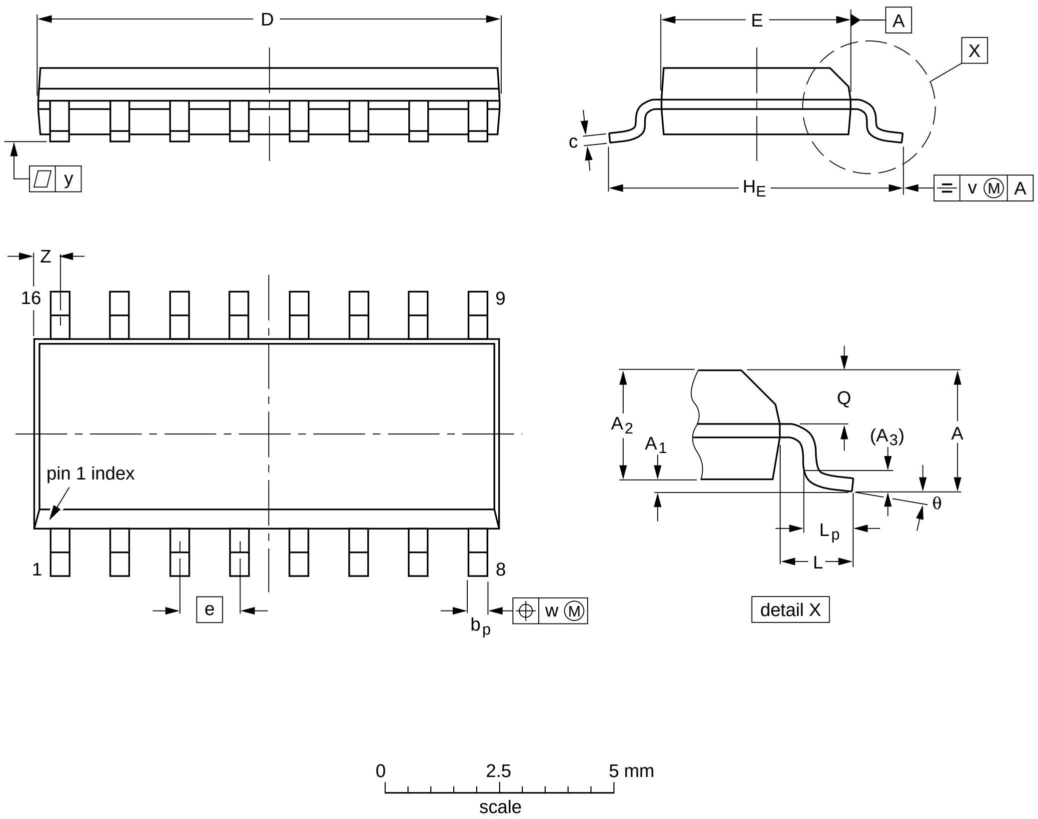


Fig 16. Test circuit for measuring sine-wave distortion

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 21. Package outline SOT109-1 (SO16)