FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13703-2E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90540/545 Series

MB90F543/F549/V540

■ DESCRIPTION

The MB90540/545 series with FULL-CAN*1 and FLASH ROM is specially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces (one for MB90V545 series), which conform to V2.0 Part A and Part B, supporting very flexible message buffer scheme and so offering more functions than a normal full CAN approach. The instruction set by F²MC-16LX CPU core inherits an AT architecture of the F²MC*2 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions.The micro controller has a 32-bit accumulator for processing long word data.The MB90540/545 series has peripheral resources of 8/10-bit A/D converters, UART(SCI), extended I/O serial interfaces, 8/16-bit timer, I/O timer (input capture(ICU), output compare (OCU)).

*1:Controller Area Network (CAN) - License of Robert Bosch GmbH.

*2:F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from: divided-by-2 of oscillation or one to four times the oscillation
  Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0V)
  Subsystem Clock: 32 kHz

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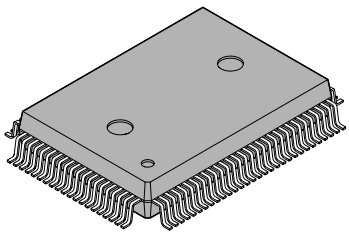
■ PACKAGE

100-pin Plastic QFP



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- Instruction set to optimize controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte Instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI^{2}OS)
- Embedded ROM size and types
  Flash ROM: 128 Kbytes / 256 Kbytes
  Embedded RAM size: 6 Kbytes / 8 Kbytes (evaluation chip)
- Flash ROM
  Supports automatic programming, Embedded Algorithm TM*
  Write / Erase / Erase-Suspend / Resume commands
  A flag indicating completion of the algorithm
  Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
  Erase can be performed on each block
  Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Clock mode
  Hardware stand-by mode
- Process
  0.5 µm CMOS technology
- I/O port
  General-purpose I/O ports: 81 ports
- Timer
  Watchdog timer: 1 channel
  8/16-bit PPG timer: 8/16-bit × 4 channels
  16-bit re-load timer: 2 channels
- 16-bit I/O timer
  16-bit free-run timer: 1 channel
  Input capture: 8 channels
  Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART 0
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized (with start/stop bit) transmission can be selectively used.

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- UART 1
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized serial (extended I/O serial) can be used.
- External interrupt circuit (8 channels)
  A module for starting an extended intelligent I/O service (EI^{2}OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution can be selectively used.
  Starting by an external trigger input.
  Conversion time: 26.3 µs
- FULL-CAN interfaces
  MB90540 series: 2 channel
  MB90545 series: 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface: Maximum address space 16 Mbytes

*: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP

The following table provides a quick outlook of the MB90540/545 Series

Features		MB90F543	MB90F549	MB90V540
Classification		Flash ROM product		Evaluation product
ROM size		128 Kbytes Boot Block	256 Kbytes Boot Block	None
ROM size		6 K		8 K
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 µs (at machine clock frequency of 16 MHz, minimum value)		
UART 0		Clock synchronized transmission (500 K / 1M / 2 Mbps) Clock asynchronized transmission (4808 / 5208 / 9615 / 10417 / 19230 / 38460 / 62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART 1 (SCI)		Clock synchronized transmission (62.5 K/ 12 K/ 250 K/ 500 K/ 1 Mbps) Clock asynchronized transmission (1202/ 2404/ 4808/ 9615/ 31250 bps) Transmission can be performed by bi-directional serial Transmission or by master / slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or mode successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers		Number of channels: 8/16 bit × 4 channels PPG operation of 8-bit or 16 bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, 128 µs (at oscillation of 4 MHz, fsys = machine clock frequency of 16 MHz, fosc = oscillation clock frequency)		
16-bit Reload timer		Number of channels:2 Operation clock frequency: fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 8 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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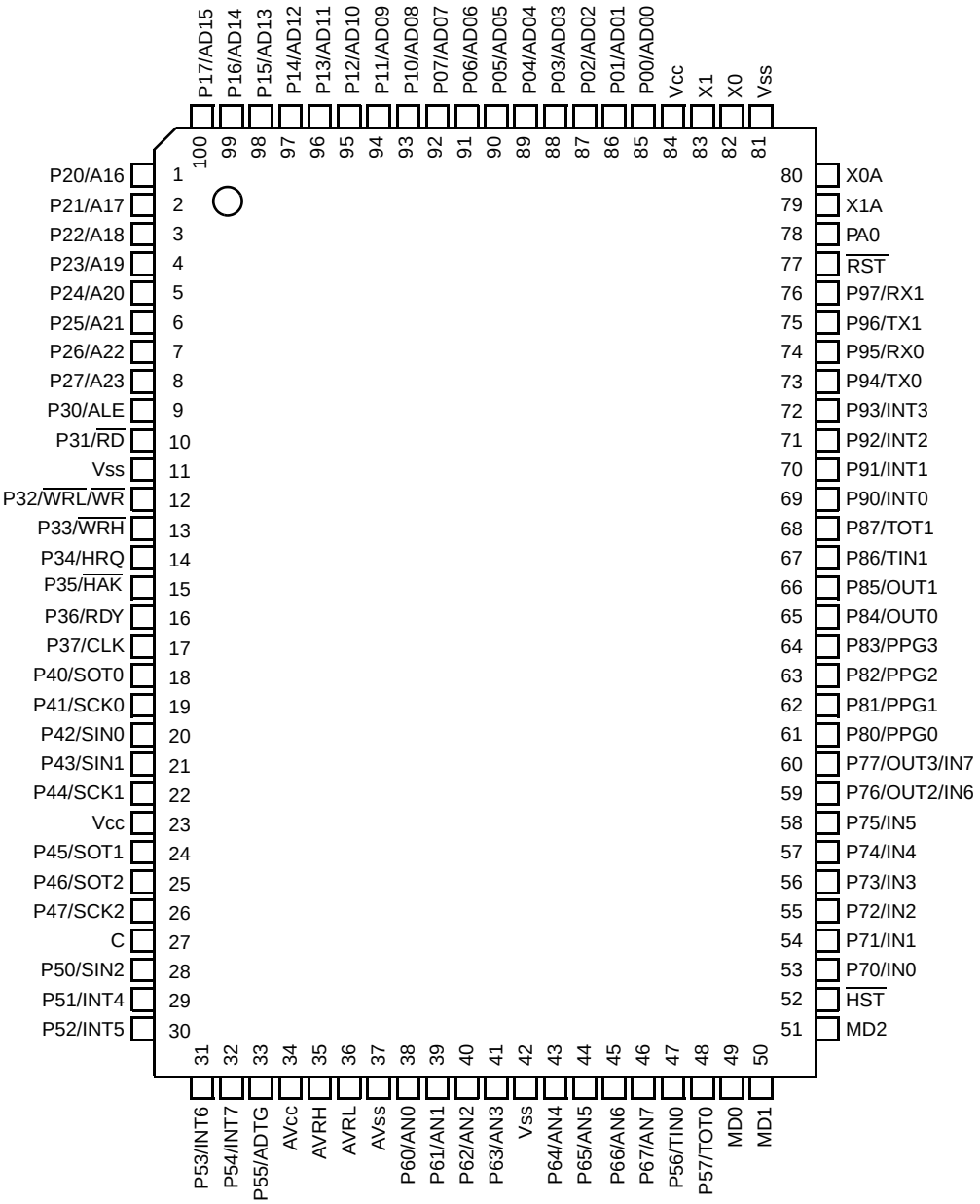
Features	MB90F543	MB90F549	MB90V540
CAN Interface	Number of channels: 2(MB90540 series), 1(MB90545 series) Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1 Mbps		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Extended I/O serial interface	Clock synchronized transmission (31.25 K / 62.5 K /125 K / 500 K / 1 Mbps at machine clock frequency of 16 MHz) LSB first / MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm ™ and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/ stop/ CPU intermittent operation/ clock timer/ hardware stand-by		
Process	CMOS		
Power supply voltage for operation	5 V ± 10 %		
Package	QFP-100		PGA-256

*: Varies with conditions such as operating frequency. (See section " ■ Electrical Characteristics".)

■ PIN ASSIGNMENT

(Top view)



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■ PIN DESCRIPTION

No.	Pin name	Circuit type	Function
82 83	X0 X1	A (Oscillation)	High speed oscillator input pins
80 79	X0A X1A	A (Oscillation)	Low speed oscillator input pins
77	$\overline{RST}$	B	External reset request input
52	$\overline{HST}$	C	Hardware standby input
85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
1 to 8	P20 to P27	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	A16 to A23		8-bit I/O pins for A16 to A23 at the external address bus. This function is enabled when the external bus is enabled.
9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	$\overline{RD}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{WR}$/$\overline{WRL}$ pin output is disabled.
	$\overline{WRL}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{WR}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
	$\overline{WR}$		
13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or external bus 8-bit mode or when $\overline{WRH}$ pin output is disabled.
	$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

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No.	Pin name	Circuit type	Function
14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the clock output is disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
19	P41	G	General I/O port. This function is enabled when UART0 disables clock output.
	SCK0		Clock I/O pin for UART0. This function is enabled when UART0 enables the clock output.
20	P42	G	General I/O port. This function is always enabled.
	SIN0		Serial data input pin for UART0. While UART0 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
21	P43	G	General I/O port. This function is always enabled.
	SIN1		Serial data input pin for UART1. While UART1 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
	SCK1		Clock pulse input/output pin for UART1. This function is enabled when UART1 enables the clock output.
24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
	SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.

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No.	Pin name	Circuit type	Function
25	P46	G	General I/O port. This function is enabled when the Serial IO disables the serial data output.
	SOT2		Serial data output pin for the Serial IO. This function is enabled when the Serial IO enables the serial data output.
26	P47	G	General I/O port. This function is enabled when the Serial IO disables the clock output.
	SCK2		Clock pulse input/output pin for the Serial IO. This function is enabled when the Serial IO enables the clock output.
28	P50	D	General I/O port. This function is always enabled.
	SIN2		Serial data input pin for the Serial IO. While the Serial IO is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
	INT4 to INT7		External interrupt request input pins for INT4 to INT7. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
33	P55	D	General I/O port. This function is always enabled.
	ADTG		Trigger input pin for the A/D converter. While the A/D converter is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
	AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
	AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
47	P56	D	General I/O port. This function is always enabled.
	TIN0		Event input pin for the 16-bit reload timers 0. While the 16-bit reload timer is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.

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No.	Pin name	Circuit type	Function
53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
	IN0 to IN5		Data sample input pins for input captures ICU0 to ICU5. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
59 to 60	P76 to P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT2 to OUT3		Waveform output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
	IN6 to IN7		Data sample input pin for input captures ICU6 and ICU7. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
	PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
65 to 66	P84 to P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT0 to OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
67	P86	D	General I/O port. This function is always enabled.
	TIN1		Event input pin for the 16-bit reload timers 1. While the 16-bit reload timer is operating as an input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT1		Output pin for the 16-bit reload timers 1 This function is enabled when the 16-bit reload timers 1 enables the output.
69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
	INT0 to INT3		External interrupt request input pins for INT0 to INT3. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
	TX0		TX Output pin for CAN0. This function is enabled when CAN0 enables the output.
74	P95	D	General I/O port. This function is always enabled.
	RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.

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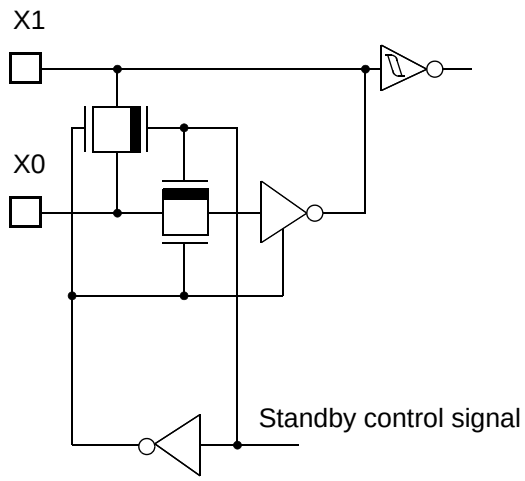
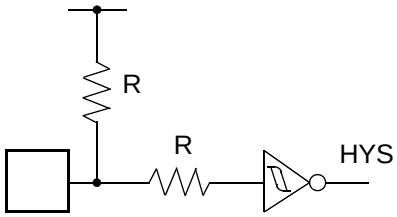
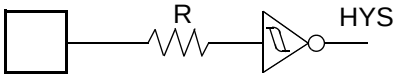
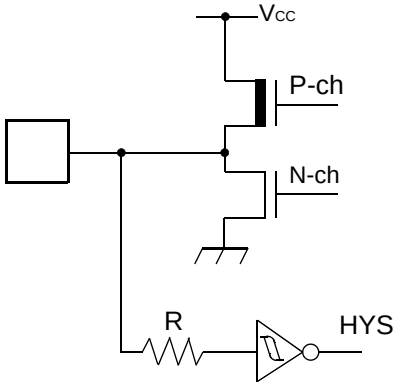
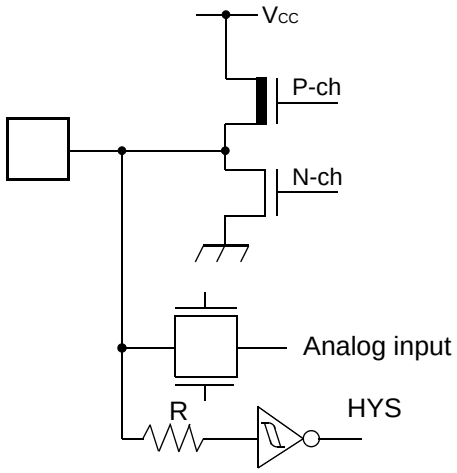
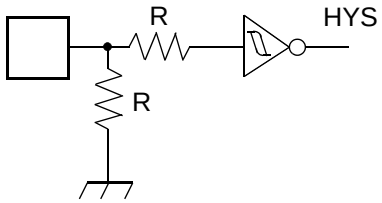
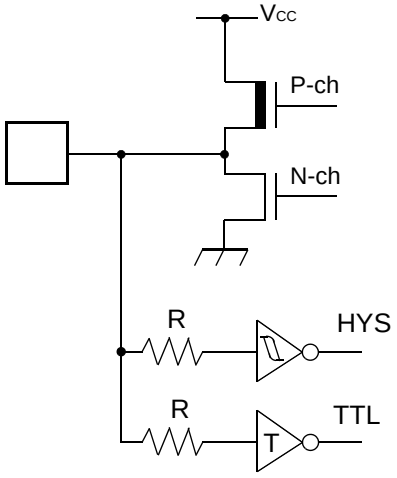
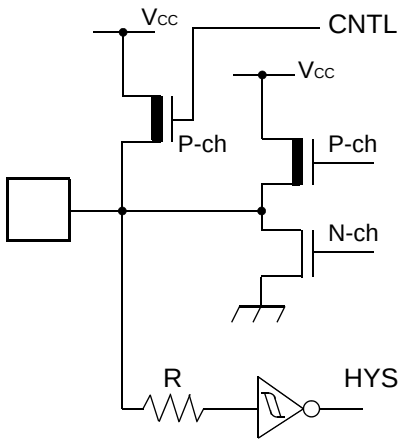
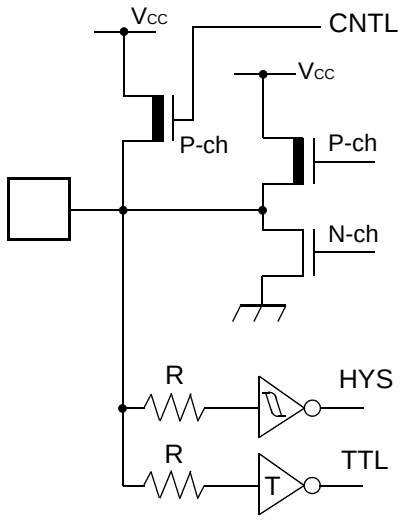
No.	Pin name	Circuit type	Function
75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
	TX1		TX Output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540 series).
76	P97	D	General I/O port. This function is always enabled.
	RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540 series).
78	PA0	D	General I/O port. This function is always enabled.
34	AV_{CC}	Power supply	Power supply for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVcc is applied to Vcc.
37	AV_{SS}	Power supply	Power supply for the A/D Converter.
35	AVRH	Power supply	External reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AVcc.
36	AVRL	Power supply	External reference voltage input for the A/D Converter.
49 50	MD0 MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to Vcc or Vss.
51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to Vcc or Vss.
27	C		This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

■ I/O CIRCUIT TYPE

Circuit type	Diagram	Remarks
A		• Oscillation feedback resistor: 1 MΩ approx.
B		• Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		• Hysteresis input
D		• CMOS level output • Hysteresis input

Circuit type	Diagram	Remarks
E		• CMOS level output • Hysteresis input • Analog input
F		• Hysteresis input • Pull-down Resistor: 50 kΩ approx. (except FLASH devices)
G		• CMOS level output • Hysteresis input • TTL input (FLASH devices only)

Circuit type	Diagram	Remarks
H		• CMOS level output • Hysteresis input • Programmable pullup resistor: 50 kΩ approx.
I		• CMOS level output • Hysteresis input • TTL level input (FLASH devices only) • Programmable pullup resistor: 50 kΩ approx.

■ HANDLING DEVICES

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than Vcc or lower than Vss is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc and Vss.
- The AVcc power supply is applied before the Vcc voltage.

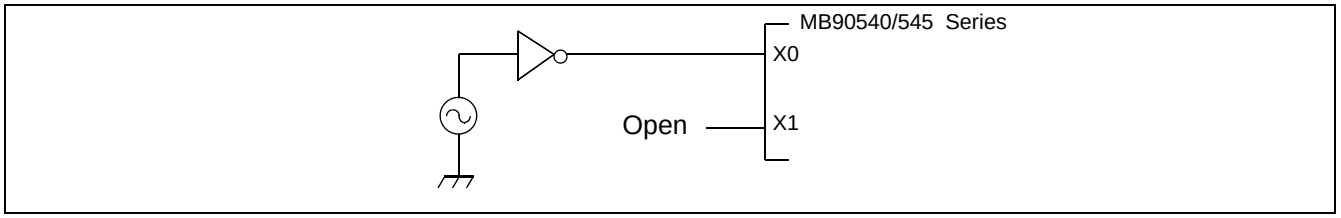
Latch-up may increase the power supply current drastically, causing thermal damage to the device.
For the same reason, care must also be taken in not allowing the analog power-supply voltage (AVcc, AVRH, DVcc) to exceed the digital power-supply voltage.

(2) Handling unused input pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.
Below is a diagram of how to use external clock.

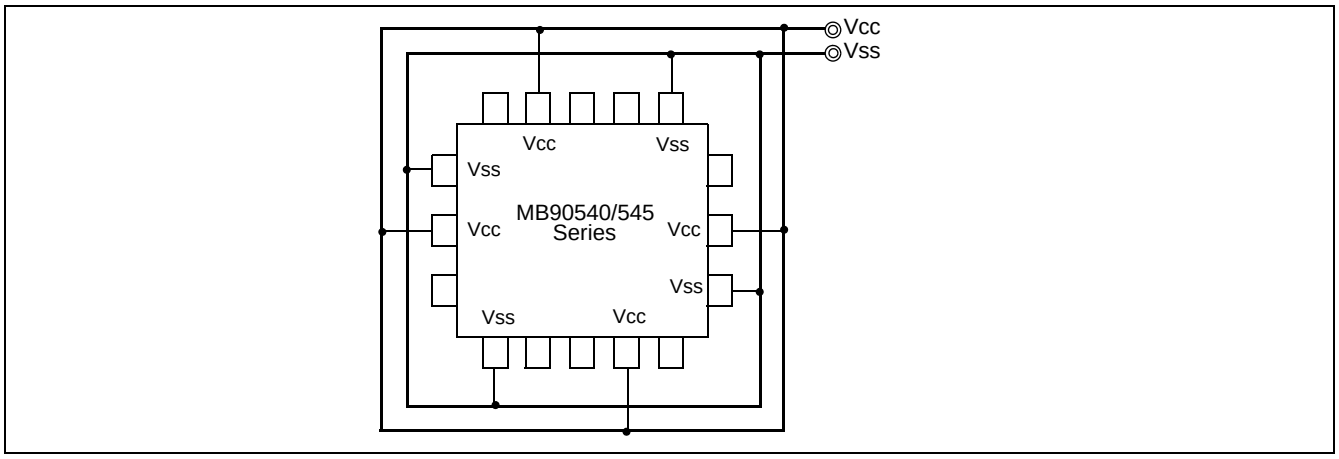


(4) Not using subclock mode

Oscillations must be connected to the X0A and X1A, even when a subclock is not used.

(5) Power supply pins (Vcc/Vss)

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 µF between V_{CC} and V_{SS} pins near the device.



(6) Pull-up/down resistors

The MB90540/545 Series does not support internal pull-up/down resistors (except Port0 - Port3:pull-up resistors). Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a grand area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

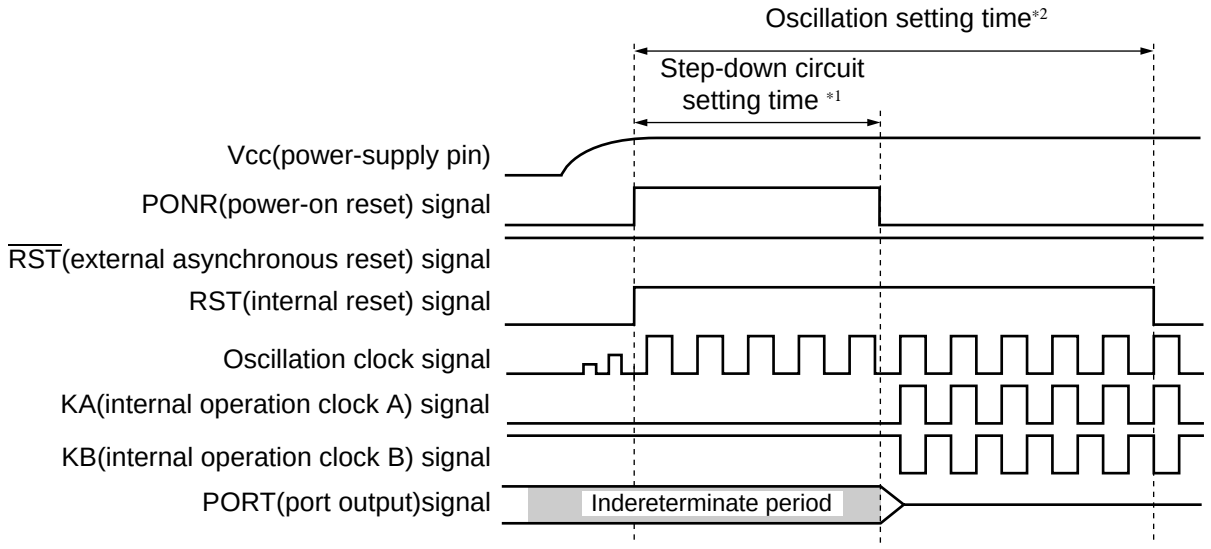
(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

(12) Indeterminate outputs from ports 0 and 1

The outputs from 0 and 1 become indeterminate during a power-on reset after the power is turned on.
Pay attention to the port output timing shown as follows.

- **Timming chart of indeterminate outputs from ports o and 1**



* : 1:Step-down circuit setting time : 2^{17}/oscillation clock frequency (oscillation clock frequency of 16 MHz: 8.19 ms)

* : 2:Oscillation setting time: 2^{18}/oscillation clock frequency (oscillation cllock frequency of 16 MHz: 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

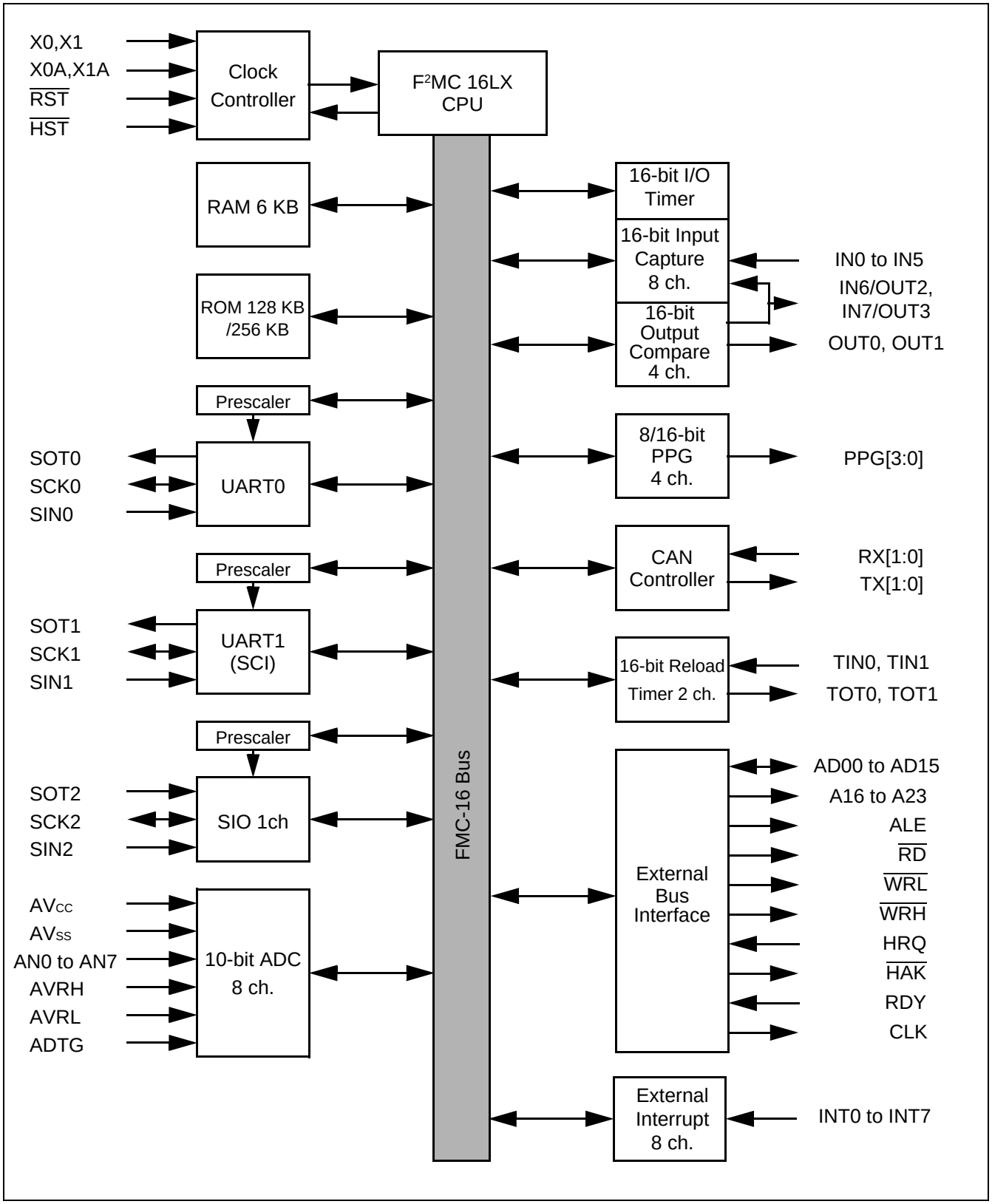
In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00h”.

If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than “00h”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

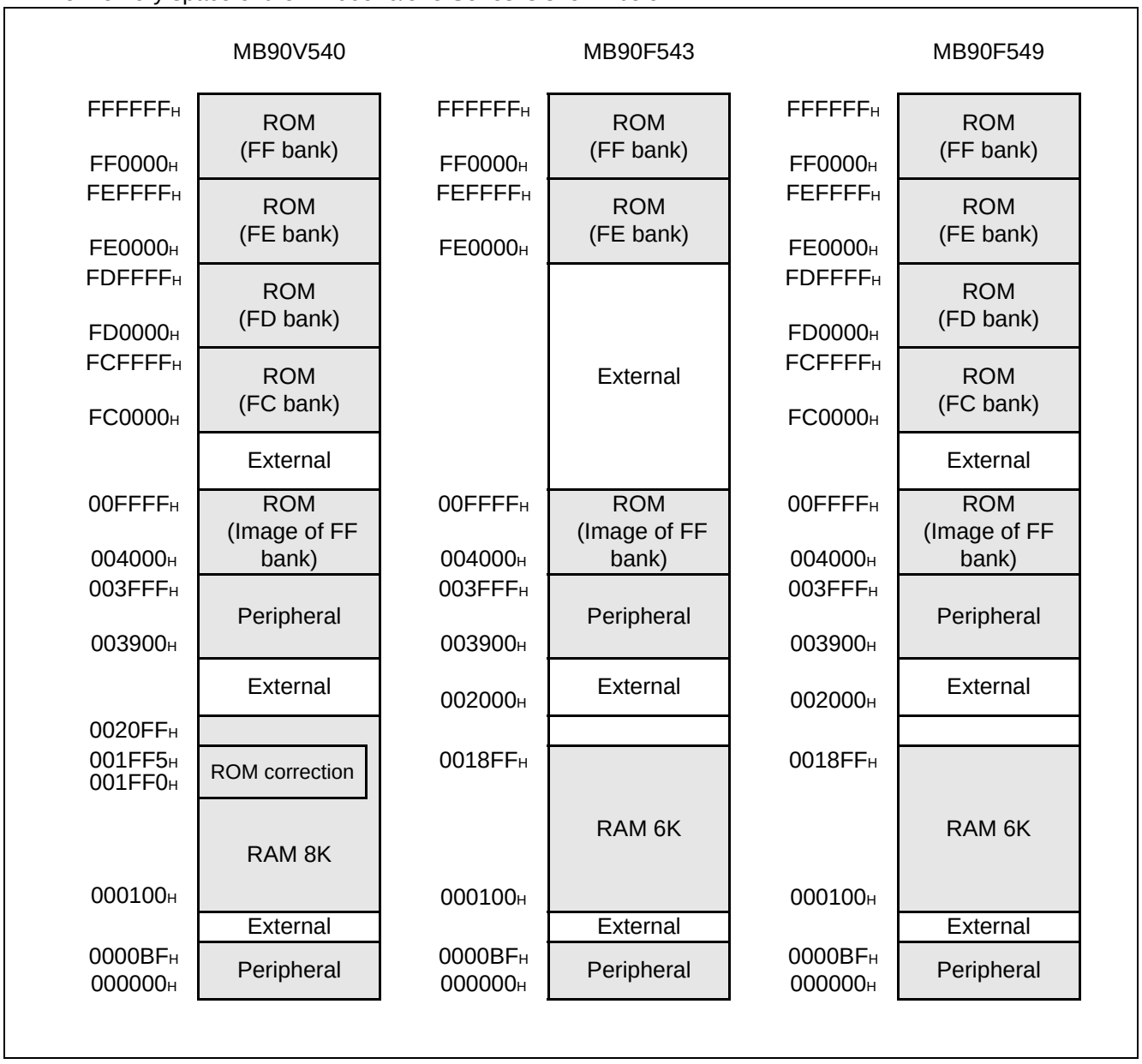
Extended intelligent I/O service (EI^{2}OS) can not be used, while REALOS is used.

■ BLOCK DIAGRAM



■ MEMORY SPACE

The memory space of the MB90540/545 Series is shown below.



The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.

For example, an attempt to access $00C000_H$ accesses the value at $FFC000_H$ in ROM.The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.The image between $FF4000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF3FFF_H$ is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Peripheral	Initial value
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
05H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
07H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
0AH	Port A data register	PDRA	R/W	Port A	_ _ _ _ _ _ _XB
0BH to 0FH	Reserved				
10H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0B
11H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0B
12H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0B
13H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0B
14H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0B
15H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0B
16H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0B
17H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0B
18H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0B
19H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0B
1AH	Port A direction register	DDRA	R/W	Port A	_ _ _ _ _ _ _0B
1BH	Analog Input Enable	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
1CH	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0B
1DH	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0B
1EH	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0B
1FH	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0B
20H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0B
21H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0B
22H	Serial Input/Output data register 0	UIDR0/ UODR0	R/W		XXXXXXXXB
23H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0XB

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial input/output data register 1	SIDR1/ SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0B
28H	UART1 prescaler control register	U1CDCR	R/W		0_ _ _1 1 1 1B
29H	Edge selector	SES1	R/W		_ _ _ _ _ _ _0B
2AH	Reserved				
2BH	Serial IO prescaler	SCDCR	R/W	Serial IO	0_ _ _1 1 1 1B
2CH	Serial mode control register	SMCS	R/W		_ _ _ _0 0 0 0B
2DH	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial data register	SDR	R/W		XXXXXXXXB
2FH	Edge selector	SES2	R/W		_ _ _ _ _ _ _0B
30H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External interrupt request register	EIRR	R/W		XXXXXXXXB
32H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D data register 0	ADCR0	R		XXXXXXXXB
37H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0 and PPG1 clock select register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2 and PPG3 Clock Select Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4 and PPG5 clock select register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6 and PPG7 output pin control register	PPG67	R/W		0 0 0 0 0 0 _ _B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
47H to 4BH	Reserved				
4CH	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0B
4DH	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0B
4EH	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0B
4FH	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0B
50H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0B
51H	Timer control status register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0B
52H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
53H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
54H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0B
55H	Timer control status register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0B
56H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
57H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
58H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0B
59H	Output compare control status register 1	OCS1	R/W		_ _ _0 0 0 0 0B
5AH	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0B
5BH	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0B
5CH to 6BH	Reserved				
6CH	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0B
6DH	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0B
6EH	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0B
6FH	ROM mirror register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1B
70H to 7FH	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
80H to 8FH	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
90H to 9DH	Reserved				
9EH	ROM correction control status register	PACSR	R/W	ROM Correction	0 0 0 0 0 0 0 0B
9FH	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0B
A0H	Low-power mode register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0B
A1H	Clock selector register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0B
A2H to A4H	Reserved				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
A5H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0B
A6H	External address output control register	HACR	W		0 0 0 0 0 0 0 0B
A7H	Bus control signal select register	ECSR	W		0 0 0 0 0 0 0 _B
A8H	Watchdog control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1B
A9H	Time Base Timer Control	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0B
AAH	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0B
ABH to ADH	Reserved				
AEH	Flash control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 _ _ 0B
AFH	Reserved				
B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
B1H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1B
B2H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1B
B3H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1B
B4H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1B
B5H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1B
B6H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1B
B7H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1B
B8H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1B
B9H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1B
BAH	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1B
BBH	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1B
BCH	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1B
BDH	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1B
BEH	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1B
BFH	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1B
COH to FFH	External				

Address	Register	Abbreviation	Access	Peripheral	Initial value
1FF0H	ROM Correction Address 0	PADR0	R/W	ROM correction	XXXXXXXXB
1FF1H	ROM Correction Address 1	PADR0	R/W		XXXXXXXXB
1FF2H	ROM Correction Address 2	PADR0	R/W		XXXXXXXXB
1FF3H	ROM Correction Address 3	PADR1	R/W		XXXXXXXXB
1FF4H	ROM Correction Address 4	PADR1	R/W		XXXXXXXXB
1FF5H	ROM Correction Address 5	PADR1	R/W		XXXXXXXXB

Address	Register	Abbreviation	Access	Peripheral	Initial value
3900H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
3901H	Reload H	PRLH0	R/W		XXXXXXXXB
3902H	Reload L	PRLL1	R/W		XXXXXXXXB
3903H	Reload H	PRLH1	R/W		XXXXXXXXB
3904H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
3905H	Reload H	PRLH2	R/W		XXXXXXXXB
3906H	Reload L	PRLL3	R/W		XXXXXXXXB
3907H	Reload H	PRLH3	R/W		XXXXXXXXB
3908H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
3909H	Reload H	PRLH4	R/W		XXXXXXXXB
390AH	Reload L	PRLL5	R/W		XXXXXXXXB
390BH	Reload H	PRLH5	R/W		XXXXXXXXB
390CH	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
390DH	Reload H	PRLH6	R/W		XXXXXXXXB
390EH	Reload L	PRLL7	R/W		XXXXXXXXB
390FH	Reload H	PRLH7	R/W		XXXXXXXXB
3910H to 3917H	Reserved				
3918H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
3919H	Input Capture 0	IPCP0	R		XXXXXXXXB
391AH	Input Capture 1	IPCP1	R		XXXXXXXXB
391BH	Input Capture 1	IPCP1	R		XXXXXXXXB
391CH	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
391DH	Input Capture 2	IPCP2	R		XXXXXXXXB
391EH	Input Capture 3	IPCP3	R		XXXXXXXXB
391FH	Input Capture 3	IPCP3	R		XXXXXXXXB
3920H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
3921H	Input Capture 4	IPCP4	R		XXXXXXXXB
3922H	Input Capture 5	IPCP5	R		XXXXXXXXB
3923H	Input Capture 5	IPCP5	R		XXXXXXXXB
3924H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
3925H	Input Capture 6	IPCP6	R		XXXXXXXXB
3926H	Input Capture 7	IPCP7	R		XXXXXXXXB
3927H	Input Capture 7	IPCP7	R		XXXXXXXXB

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
3928H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3B00H to 3BFFH	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3C00H to 3CFFH	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3D00H to 3DFFH	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3E00H to 3FFFH	Reserved				

Note Initial value of “_” represents unused bit, “X” represents unknown value.
Addresses in the range 0000H to 00FFH, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in an “X” reading and any write access should not be performed.

■ CAN CONTROLLER

The MB90540 series contains two CAN controllers (CAN0 and CAN1), the MB90545 series contains only one (CAN0). The Evaluation Chip MB90V540 also has two CAN controllers.
The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 1 Mbit/s (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070H	000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000071H	000081H				
000072H	000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000073H	000083H				
000074H	000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000075H	000085H				
000076H	000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000077H	000087H				
000078H	000088H	Receive complete register	RCR	R/W	00000000 00000000B
000079H	000089H				
00007AH	00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00007BH	00008BH				
00007CH	00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00007DH	00008DH				
00007EH	00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00007FH	00008FH				

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00H	003D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
003B01H	003D01H				
003B02H	003D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
003B03H	003D03H				
003B04H	003D04H	Receive/transmit error counter	RTEC	R	00000000 00000000B
003B05H	003D05H				
003B06H	003D06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H				
003B08H	003D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H				
003B0AH	003D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH				
003B0CH	003D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH				
003B0EH	003D0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH				
003B10H	003D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H				
003B12H	003D12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H				
003B14H	003D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H				
003B16H	003D16H				XXXXX--- XXXXXXXXB
003B17H	003D17H				
003B18H	003D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H				
003B1AH	003D1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH				

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00H to 003A1FH	003C00H to 003C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
003A21H	003C21H				
003A22H	003C22H				XXXXX--- XXXXXXXXB
003A23H	003C23H				
003A24H	003C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
003A25H	003C25H				
003A26H	003C26H				XXXXX--- XXXXXXXXB
003A27H	003C27H				
003A28H	003C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
003A29H	003C29H				
003A2AH	003C2AH				XXXXX--- XXXXXXXXB
003A2BH	003C2BH				
003A2CH	003C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
003A2DH	003C2DH				
003A2EH	003C2EH				XXXXX--- XXXXXXXXB
003A2FH	003C2FH				
003A30H	003C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
003A31H	003C31H				
003A32H	003C32H				XXXXX--- XXXXXXXXB
003A33H	003C33H				
003A34H	003C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
003A35H	003C35H				
003A36H	003C36H				XXXXX--- XXXXXXXXB
003A37H	003C37H				
003A38H	003C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
003A39H	003C39H				
003A3AH	003C3AH				XXXXX--- XXXXXXXXB
003A3BH	003C3BH				

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
003A88H to 003A8FH	003C88H to 003C8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003A90H to 003A97H	003C90H to 003C97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003A98H to 003A9FH	003C98H to 003C9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
003AA0H to 003AA7H	003CA0H to 003CA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
003AA8H to 003AAFH	003CA8H to 003CAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
003AB0H to 003AB7H	003CB0H to 003CB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003AB8H to 003ABFH	003CB8H to 003CBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	003CC0H to 003CC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	003CC8H to 003CCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
003AD0H to 003AD7H	003CD0H to 003CD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	003CD8H to 003CDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	003CE0H to 003CE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	003CE8H to 003CEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	003CF0H to 003CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	003CF8H to 003CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT MAP

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
I/O Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note:
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value		Units	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/AVRL, AVRH ≥ AVRL *1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Clamp Current	I_{CLAMP}	– 2.0	2.0	mA	
"L" level max. output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max. overall output current	$\sum I_{OL}$	—	100	mA	
"L" level avg. overall output current	$\sum I_{OLAV}$	—	50	mA	*5
"H" level max. output current	I_{OH}	—	–15	mA	*3
"H" level avg. output current	I_{OHAV}	—	–4	mA	*4
"H" level max. overall output current	$\sum I_{OH}$	—	–100	mA	
"H" level avg. overall output current	$\sum I_{OHAV}$	—	–50	mA	*5
Power consumption	P_D	—	500	mW	MB90F543/F549
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1: AV_{CC}, AVRL and AVRL should not exceed V_{CC}, and AVRL should not exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Units	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40		+85	°C	

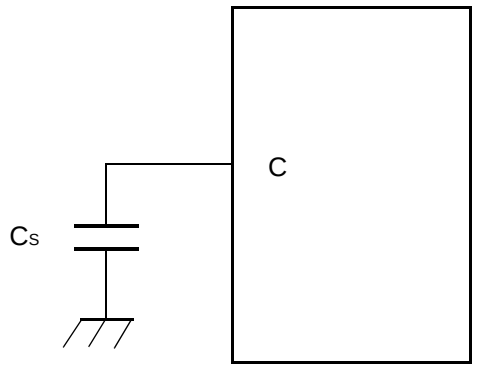
*: Use a ceramic capacitor or a capacitor of better AC characteristics. The V_{CC} Capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

- **C Pin Connection Diagram**



3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Units	Remarks
				Min.	Typ.	Max.		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{CC} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5V, I_{OH} = –4.0mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5V, I_{OL} = 4.0mA	—	—	0.4	V	
Input leak current	I_{IL}		V_{CC} = 5.5V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At normal operation	—	45	60	mA	MB90F543/F549
	I_{CCS}		V_{CC} = 5.0V±10%, Internal frequency: 16 MHz, At sleep	—	13	22	mA	MB90F543/F549
	I_{CCL}		V_{CC} = 5.0V, Internal frequency: 8 kHz, At sub operation	—	0.2	1	mA	MB90F543/F549
	I_{CCLS}		V_{CC} = 5.0V, Internal frequency: 8 kHz, At sub sleep	—	10	50	µA	MB90F543/F549
	I_{CCT}		V_{CC} = 5.0V, Internal frequency: 8 kHz, At watch mode	—	10	50	µA	MB90F543/F549
	I_{CCH1}		V_{CC} = 5.0 V±10%, At stop, T_A = 25°C	—	5	20	µA	MB90F543/F549
	I_{CCH2}		V_{CC} = 5.0 V±10%, At hardware standby mode, T_A = 25°C	—	50	100	µA	MB90F543/F549
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	10	80	pF	

*: Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

4. AC Characteristics

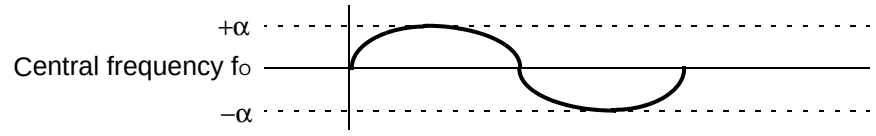
(1) Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0 V, T_A = –40 °C to +85 °C)

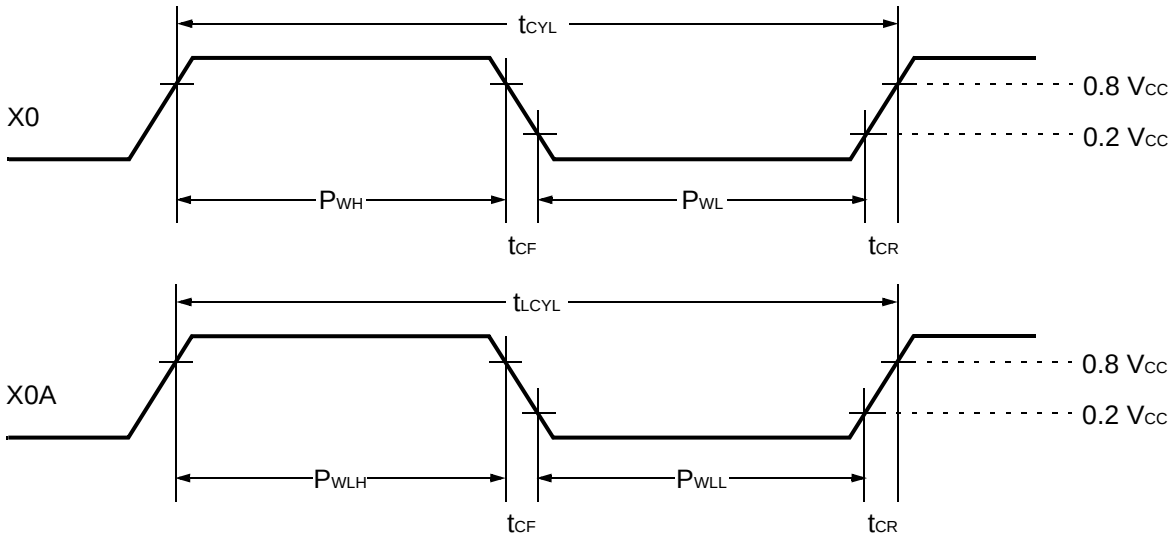
Parameter	Symbol	Pin	Value			Units	Remarks
			Min.	Typ.	Max.		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Oscillation cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
	P_{WLH},P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

* : Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

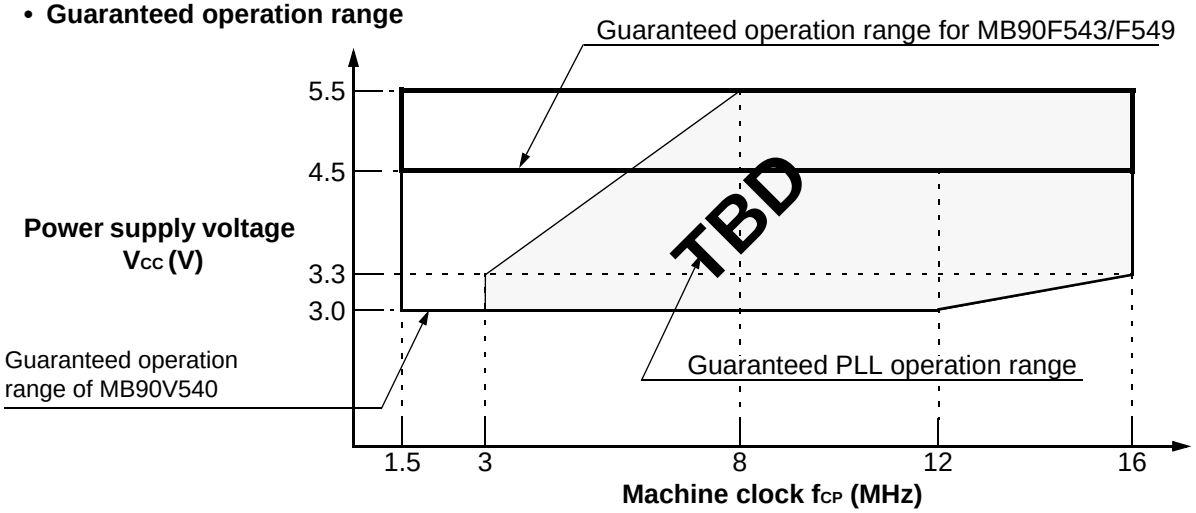
$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



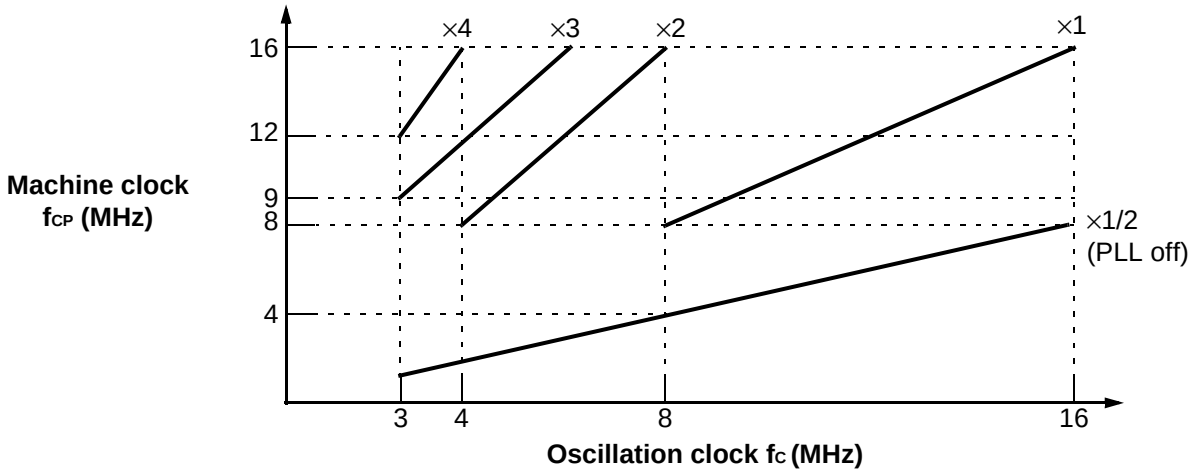
- **Clock Timing**



• **Guaranteed operation range**



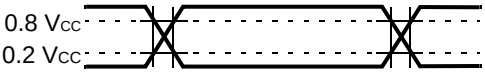
• **Oscillation clock frequency and Machine clock frequency**



AC characteristics are set to the measured reference voltage values below.

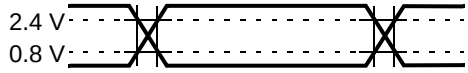
• **Input signal waveform**

Hysteresis Input Pin



• **Output signal waveform**

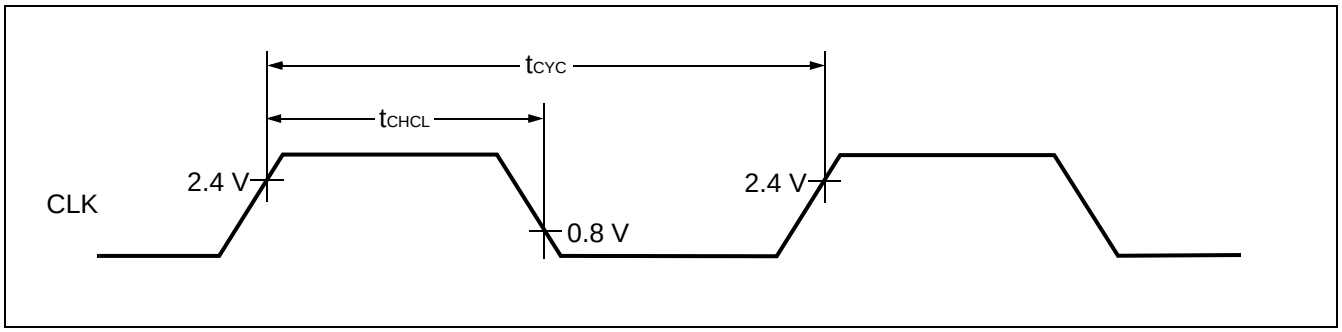
Output Pin



(2) Clock Output Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	V_{CC} = 5 V±10%	62.5	—	ns	
CLK ↑ ⇒ CLK ↓	t_{CHCL}			20	—	ns	

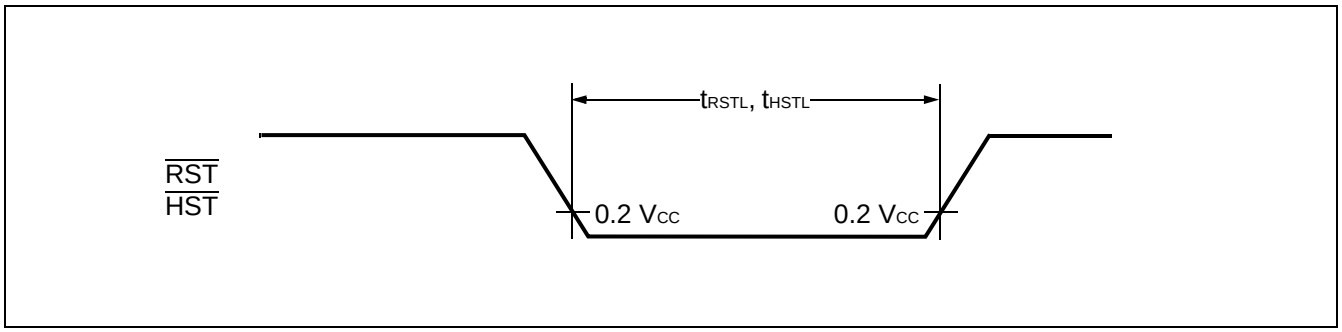


(3) Reset and Hardware Standby Input

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Value		Units	Remarks
			Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}	—	ns	

"t_{cp}" represents one cycle time of the machine clock.
Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

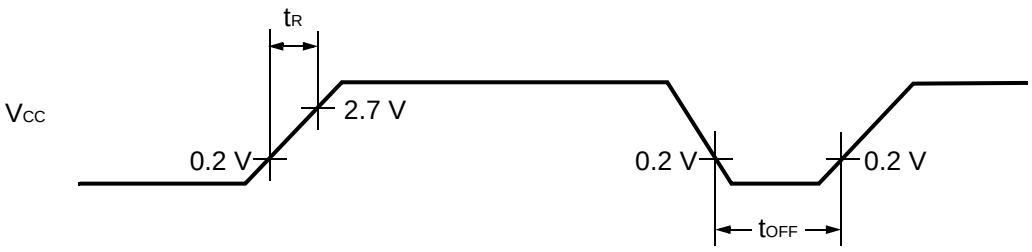


(4) Power On Reset

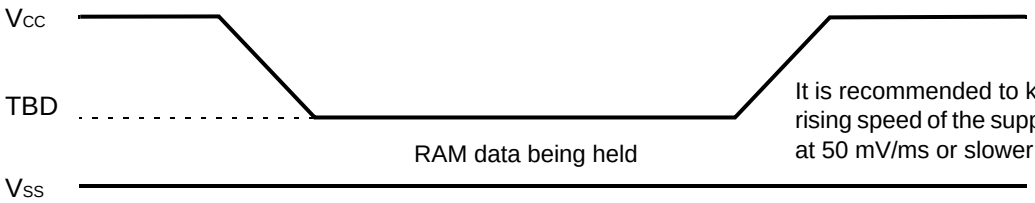
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

Note
- V_{CC} must be kept lower than 0.2 V before power-on.
- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



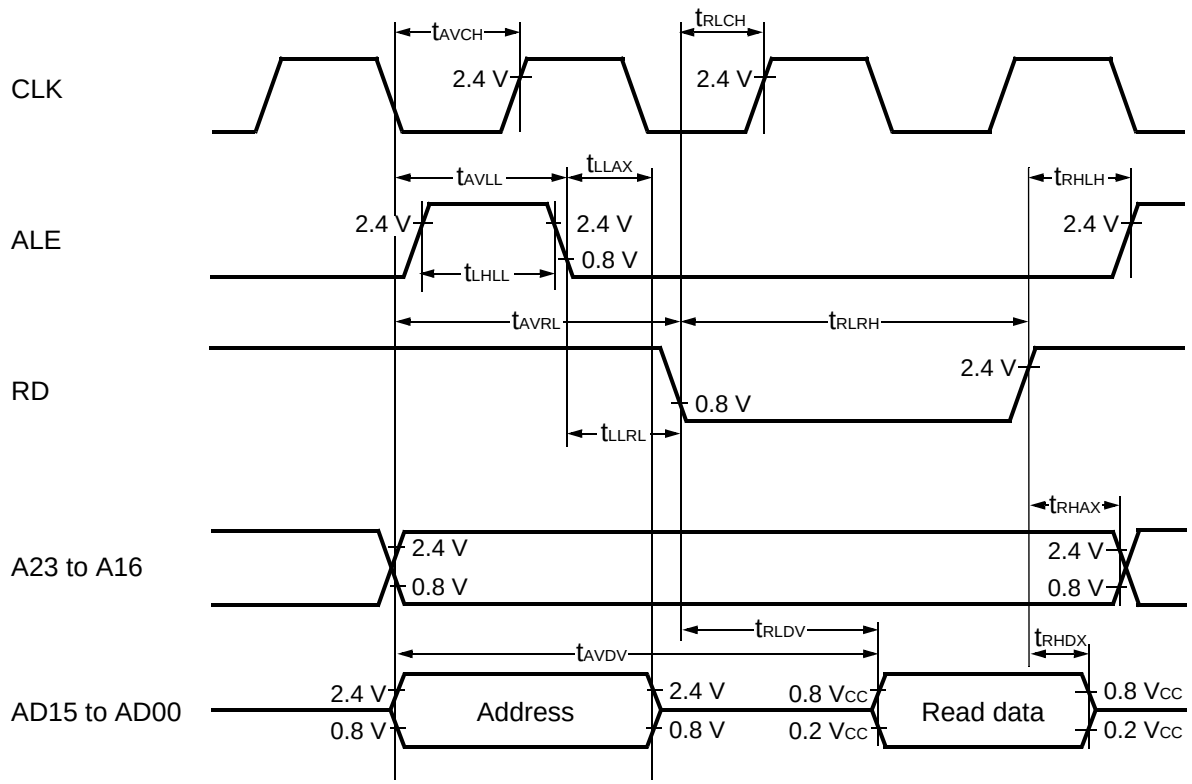
It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

(5) Bus Timing (Read)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$		ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address ⇒ $\overline{RD}$ ↓ time	t_{AVRL}	A23 toA16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$3\ t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ ⇒ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↓ ⇒ ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ ⇒ Address valid time	t_{RHAX}	$\overline{RD}$, A23 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

- **Bus Timing (Read)**

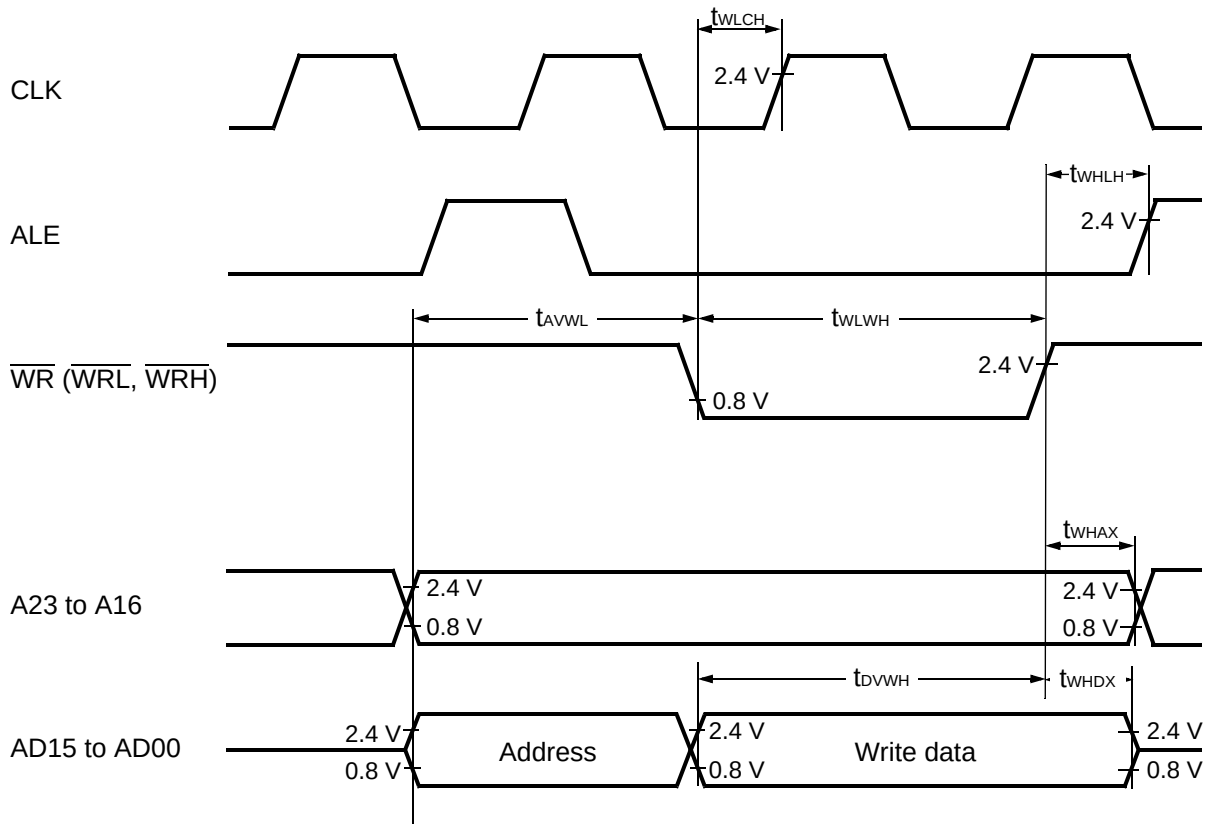


(6) Bus Timing (Write)

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Valid address ⇒ $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 – 20	—	ns	
Valid data output ⇒ $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$ ↑ ⇒ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		20	—	ns	
$\overline{WR}$ ↑ ⇒ Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ ⇒ ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ ⇒ CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 20	—	ns	

- **Bus Timing (Write)**



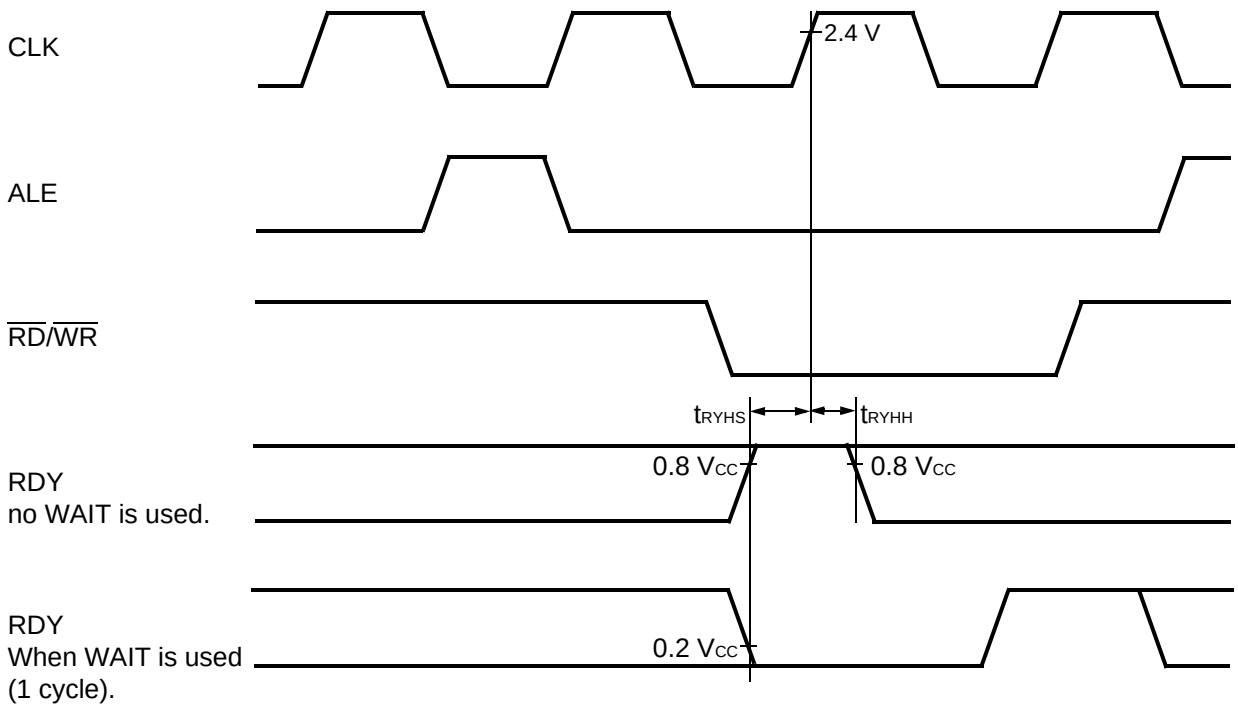
(7) Ready Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.

- **Ready Input Timing**



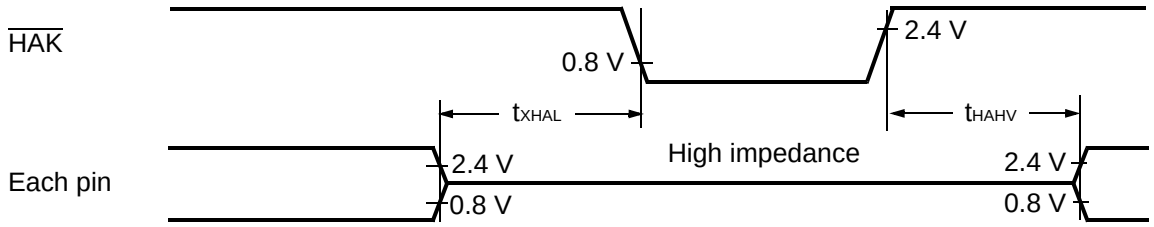
(8) Hold Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Pin floating ⇒ $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ time ⇒ Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note: There is more than 1 cycle from the time HRQ is read to the time the $\overline{HAK}$ is changed.

- **Hold Timing**



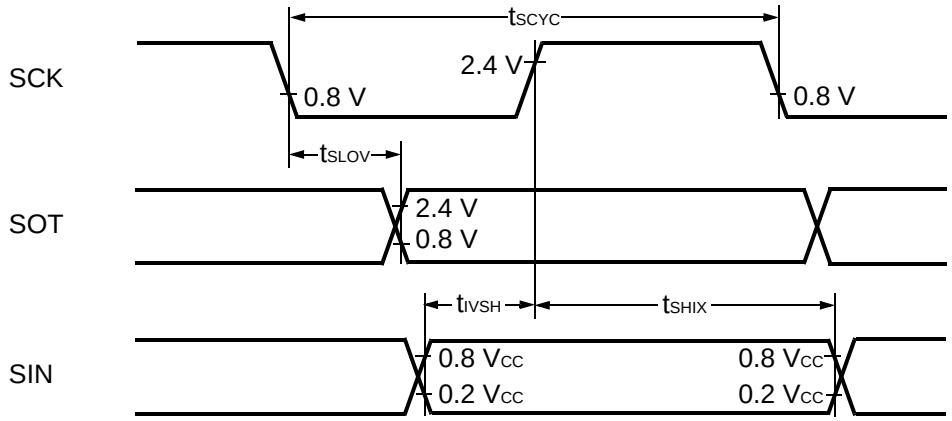
(9) UART0/1, Serial I/O Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

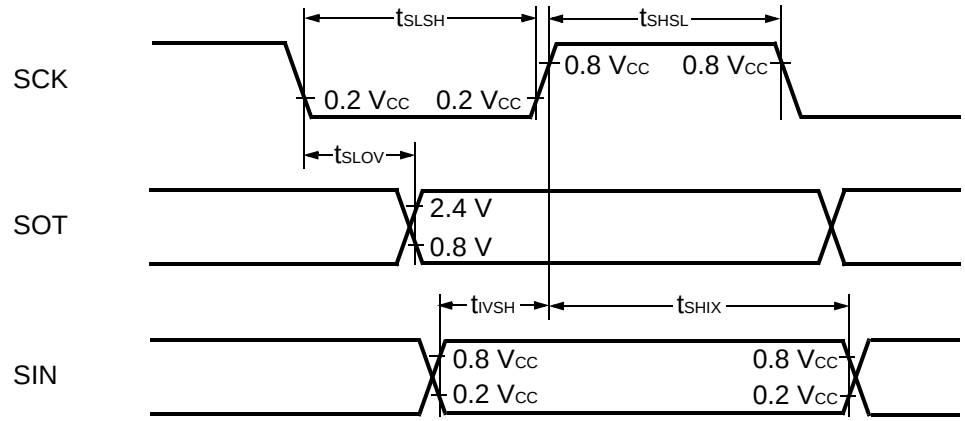
Parameter	Symbol	Pin Symbol	Condition	Value		Units	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Note: 1. AC characteristic in CLK synchronized mode.
2. C_L is load capacity value of pins when testing.
3. t_{CP} is the machine cycle (Unit: ns).

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

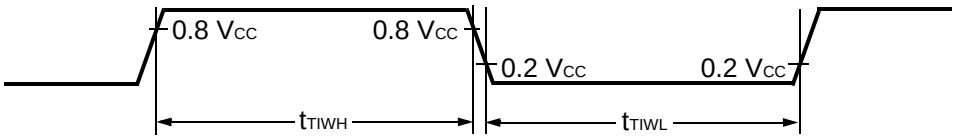


(10) Timer Related Resource Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

- **Timer Input Timing**

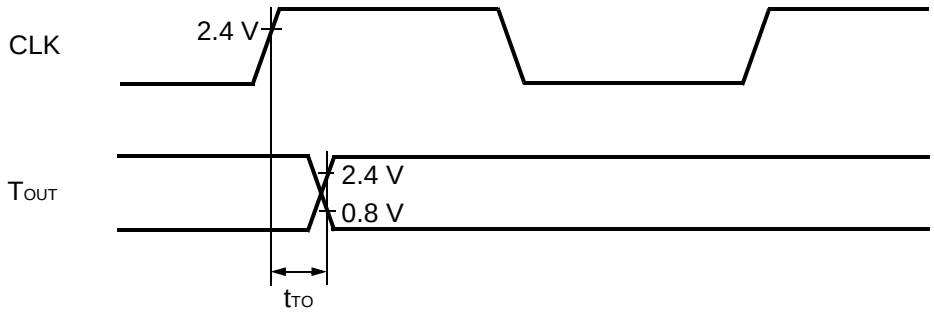


(11) Timer Related Resource Output Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
CLK ↑ ⇒ T_{OUT} change time	t_{TO}	TOT0 to TOT1, PPG0 to PPG3	—	30	—	ns	

- **Timer Output Timing**

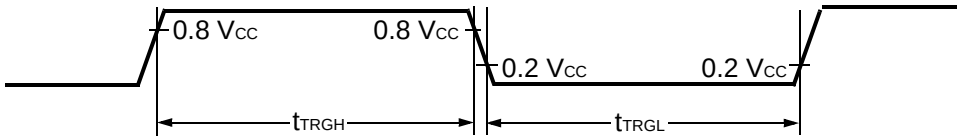


(12) Trigger Input Timing

(V_{CC} = 4.5 to 5.5 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	

- **Trigger Input Timing**



5. A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0 V,3.0 V ≤ AVRH – AVRL, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Rated Value			Units	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN7	AVRL – 3.5	AVRL + 0.5	AVRL + 4.5	mV	
Full scale reading voltage	V_{FST}	AN0 to AN7	AVRH – 6.5	AVRH – 1.5	AVRH + 1.5	mV	
Conversion time	—	—	—	$352t_{CP}$	—	ns	
Sampling time	—	—	—	$64t_{CP}$	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	–10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	200	400	600	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

*: When not using an A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

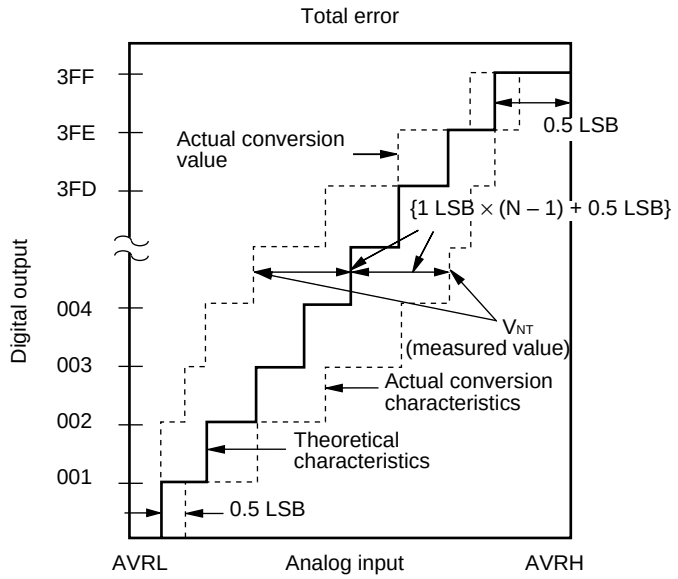
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

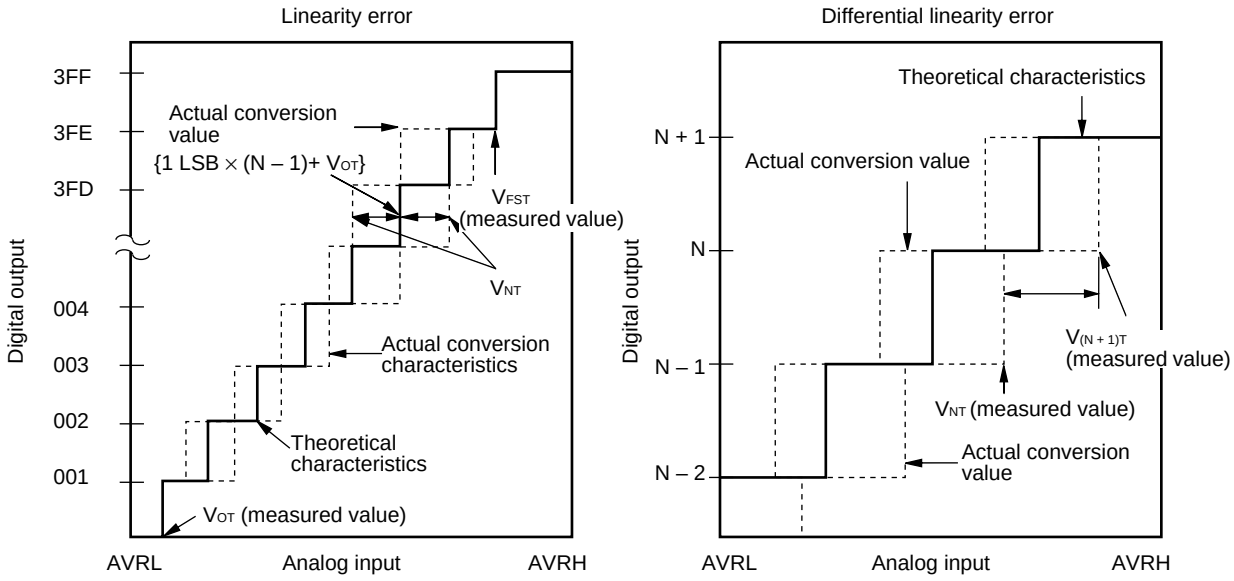
V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

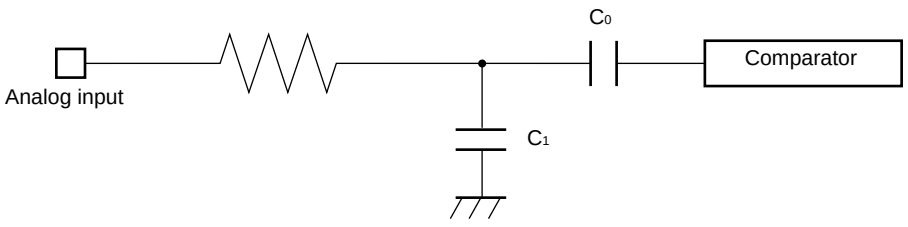
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**



Note: Listed values must be considered as standards.

- **Error**

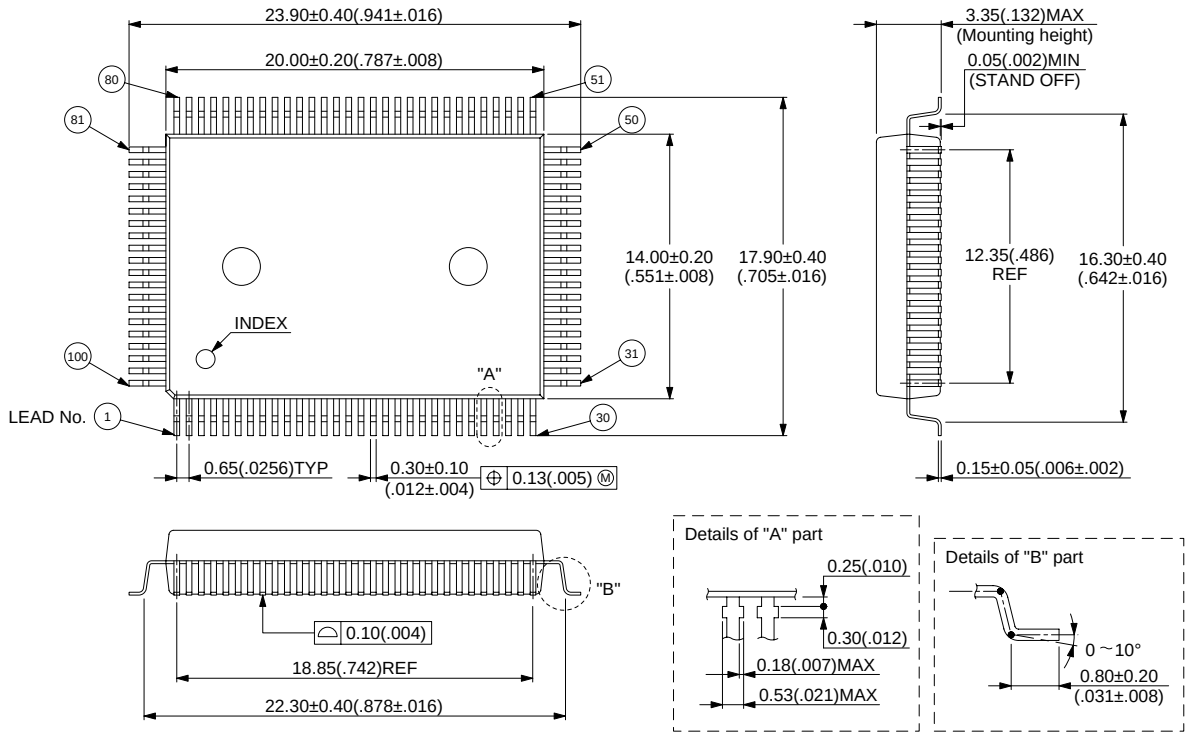
The smaller the | AVRH – AVRL |, the greater the error would become relatively.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F543PF MB90F549PF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V540CR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

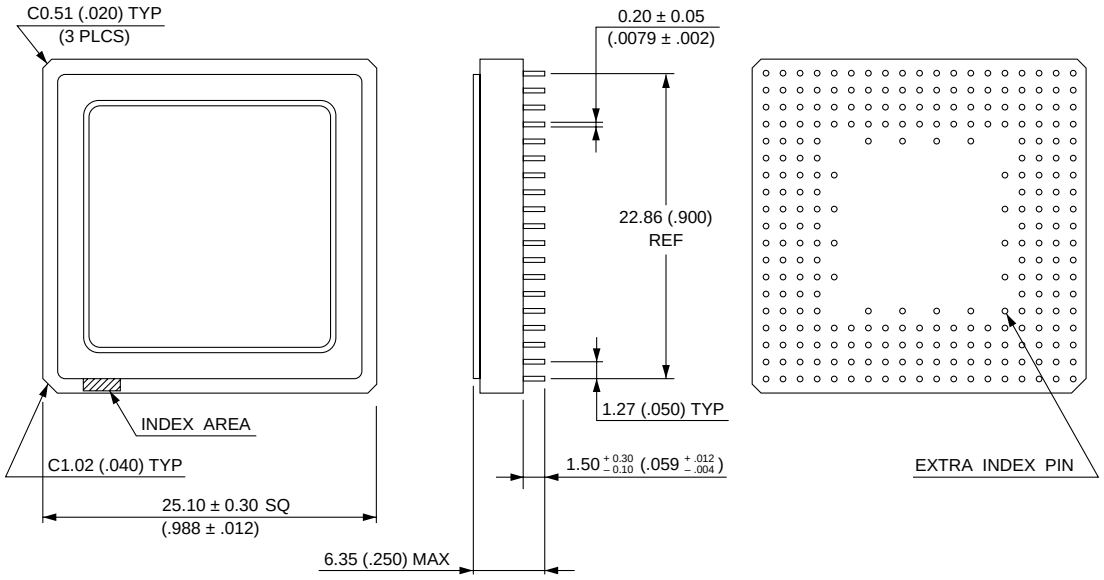
■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)



Dimensions in mm (inches)

250-pin Ceramic PGA
(PGA-256C-A01)



Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

http://edevice.fujitsu.com/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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