

## Features

- Low-voltage and Standard-voltage Operation
  - $V_{CC} = 1.7$  to  $5.5V$
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 1MHz (5.0V) and 400KHz (1.8V Compatibility)
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23 and 8-ball VFBGA
- Die Sales: Wafer Form, Waffle Pack and Bumped Wafers

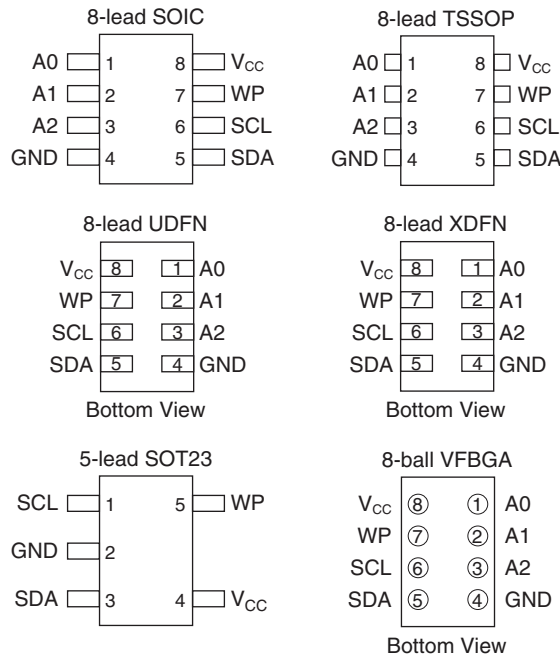
## Description

The Atmel® AT24C32D/64D provides 32,768-/65,536-bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8-bits each. The device's cascadable feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32D/64D is available in space saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23 and 8-ball VFBGA and is accessed via a 2-wire serial interface. In addition, the entire family operates from 1.7V to 5.5V.

**Table 0-1. Pin Configurations**

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

Note: For use of 5-lead SOT23, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate



## 2-Wire Serial Electrically Erasable and Programmable Read-only Memory

32K (4096 x 8)

64K (8192 x 8)

Atmel AT24C32D  
Atmel AT24C64D

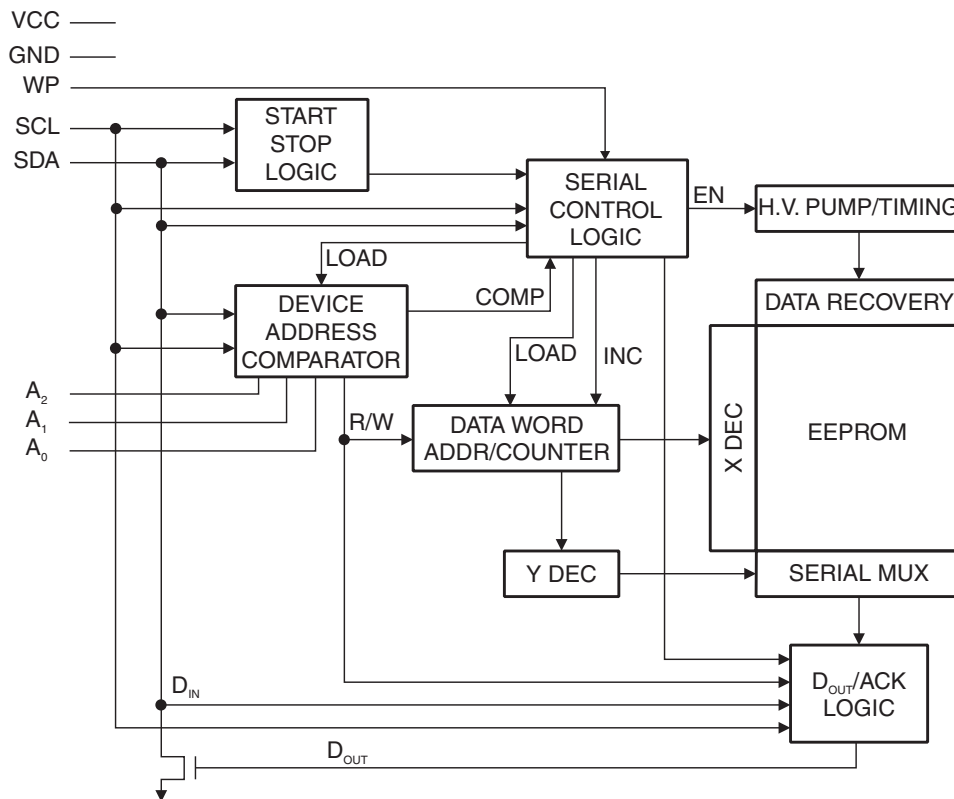


# 1. Absolute Maximum Ratings\*

Operating Temperature.....	-55 to +125°C
Storage Temperature .....	-65 to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0 to +7.0V
Maximum Operating Voltage.....	6.25V
DC Output Current .....	5.0mA

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram



## 2. Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

**DEVICE/ADDRESSES (A2, A1, A0):** The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with other Atmel® AT24CXX devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3\text{pF}$ . If coupling is  $>3\text{pF}$ , Atmel recommends connecting the address pins to GND.

**WRITE PROTECT (WP):** The write protect input, when connected to GND, allows normal write operations. When WP is connected high to  $V_{CC}$ , all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3\text{pF}$ . If coupling is  $>3\text{pF}$ , Atmel recommends connecting the pin to GND.

### 3. Memory Organization

**Atmel AT24C32D/64D, 32/64K SERIAL EEPROM:** The 32K/64K is internally organized as 128/256 pages of 32-bytes each. Random word addressing requires a 12-/13-bit data word address.

**Table 3-1.** Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{CC} = +1.7\text{V}$  to  $5.5\text{V}$

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
$C_{IN}$	Input Capacitance (A0, A1, A2, SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested

**Table 3-2.** DC Characteristics

Applicable over recommended operating range from:  $T_{AI} = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.7\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
$V_{CC1}$	Supply Voltage			1.7		5.5	V
$I_{CC1}$	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 400kHz		0.4	1.0	mA
$I_{CC2}$	Supply Current	$V_{CC} = 5.0\text{V}$	WRITE at 400kHz		2.0	3.0	mA
$I_{SB1}$	Standby Current (+1.7V option)	$V_{CC} = 1.7\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$			1.0	$\mu\text{A}$
		$V_{CC} = 5.5\text{V}$				6.0	$\mu\text{A}$
$I_{LI}$	Input Leakage Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$			0.10	3.0	$\mu\text{A}$
$I_{LO}$	Output Leakage Current $V_{CC} = 5.0\text{V}$	$V_{OUT} = V_{CC}$ or $V_{SS}$			0.05	3.0	$\mu\text{A}$
$V_{IL}$	Input Low Level <sup>(1)</sup>			-0.6		$V_{CC} \times 0.3$	V
$V_{IH}$	Input High Level <sup>(1)</sup>			$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{OL2}$	Output Low Level	$V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{mA}$			0.4	V
$V_{OL1}$	Output Low Level	$V_{CC} = 1.7\text{V}$	$I_{OL} = 0.15\text{mA}$			0.2	V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested

**Table 3-3. AC Characteristics**

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.7\text{V}$  to  $+5.5\text{V}$ ,  $CL = 1$  TTL Gate and  $100\text{pF}$  (unless otherwise noted)

Symbol	Parameter	1.7V		5.0V		Units
		Min	Max	Min	Max	
$f_{SCL}$	Clock Frequency, SCL		400		1000	kHz
$t_{LOW}$	Clock Pulse Width Low	1.3		0.4		$\mu\text{s}$
$t_{HIGH}$	Clock Pulse Width High	0.6		0.4		$\mu\text{s}$
$t_i$	Noise Suppression Time <sup>(1)</sup>		100		50	ns
$t_{AA}$	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	$\mu\text{s}$
$t_{BUF}$	Time the bus must be free before a new transmission can start <sup>(1)</sup>	1.3		0.5		$\mu\text{s}$
$t_{HD,STA}$	Start Hold Time	0.6		0.25		$\mu\text{s}$
$t_{SU,STA}$	Start Set-up Time	0.6		0.25		$\mu\text{s}$
$t_{HD,DAT}$	Data In Hold Time	0		0		$\mu\text{s}$
$t_{SU,DAT}$	Data In Set-up Time	100		100		ns
$t_R$	Inputs Rise Time <sup>(1)</sup>		0.3		0.3	$\mu\text{s}$
$t_F$	Inputs Fall Time <sup>(1)</sup>		300		100	ns
$t_{SU,STO}$	Stop Set-up Time	0.6		0.25		$\mu\text{s}$
$t_{DH}$	Data Out Hold Time	50		50		ns
$t_{WR}$	Write Cycle Time		5		5	ms
Endurance <sup>(1)</sup>	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

- Notes:
- This parameter is ensured by characterization
  - AC measurement conditions:
    - $R_L$  (connects to  $V_{CC}$ ):  $1.3\text{k}\Omega$  (2.5V, 5.0V),  $10\text{k}\Omega$  (1.7V)
    - Input pulse voltages:  $0.3 V_{CC}$  to  $0.7 V_{CC}$
    - Input rise and fall times:  $\leq 50\text{ns}$
    - Input and output timing reference voltages:  $0.5 V_{CC}$

## 4. Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to “Data Validity” diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to “Start and Stop Definition” diagram).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to “Start and Stop Definition” diagram).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

**STANDBY MODE:** The Atmel® AT24C32D/64D features a low power standby mode which is enabled:

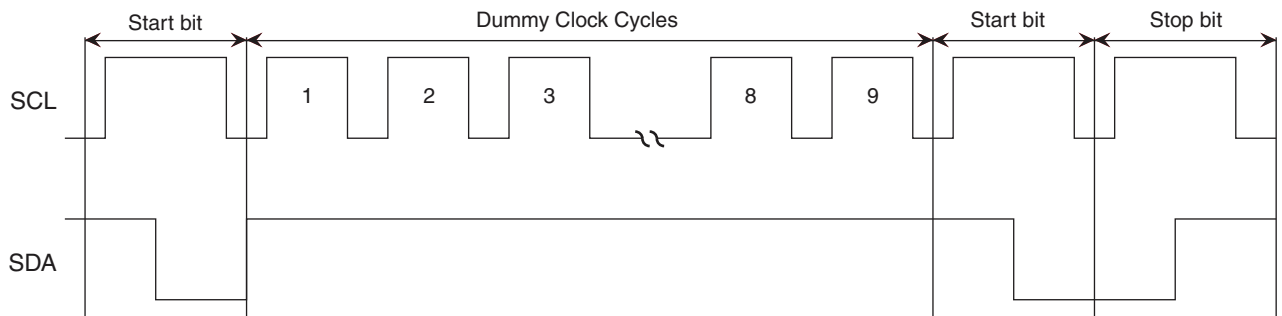
- Upon power-up
- After the receipt of the Stop bit and the completion of any internal operations.

**SOFTWARE RESET:** After an interruption in protocol, power loss or system reset, and 2-wire part can be protocol reset by following these steps:

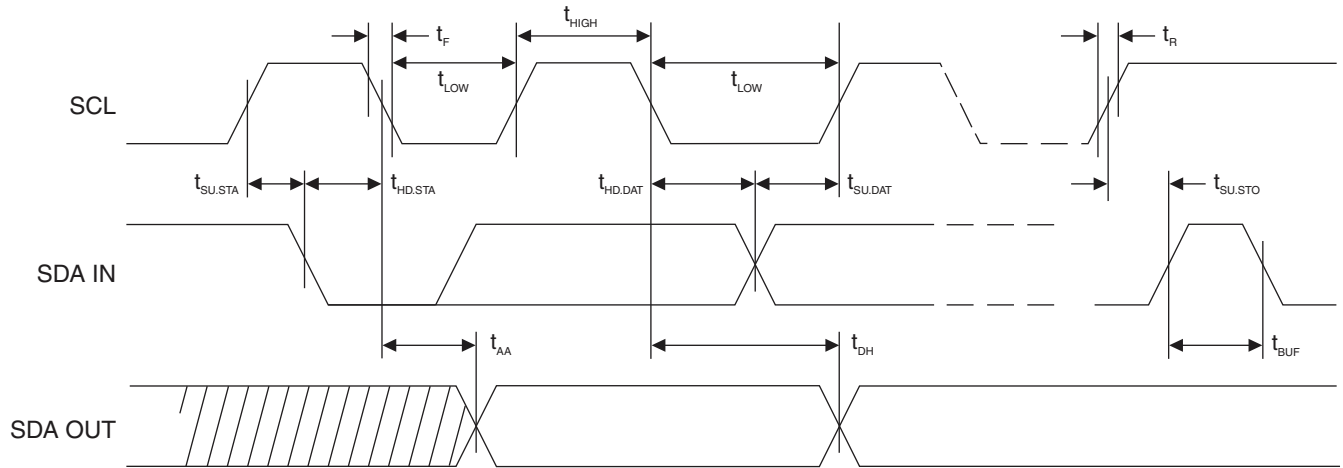
- Create a start bit condition
- Clock nine cycles
- Create another start bit followed by stop bit condition as shown below.

The device is ready for next communication after above steps have been completed.

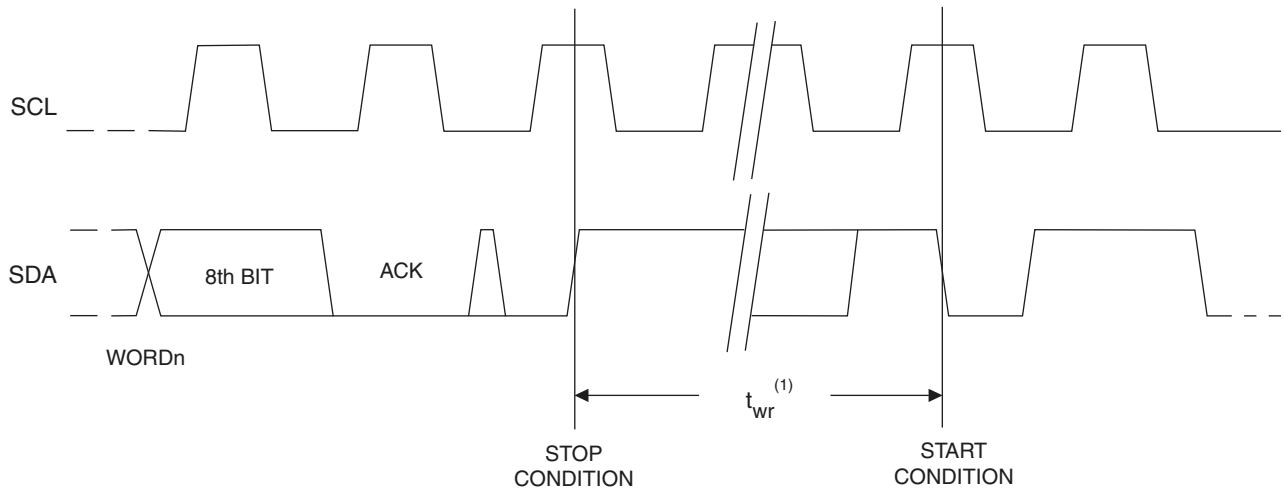
**Figure 4-1.** Software Reset



**Figure 4-2. Bus Timing**  
SCL: Serial Clock, SDA: Serial Data I/O

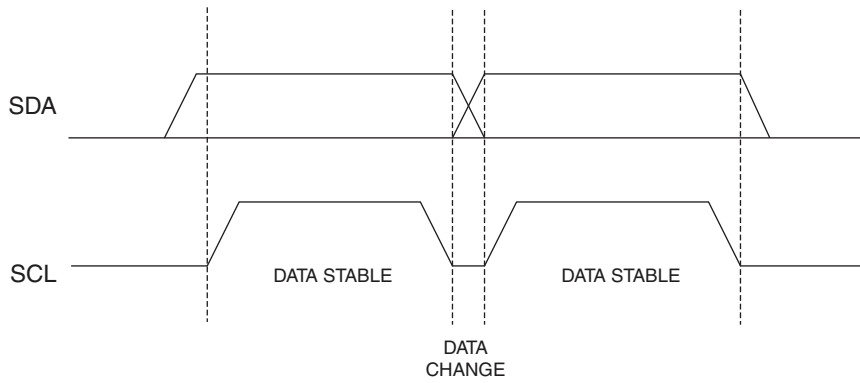


**Figure 4-3. Write Cycle Timing**  
SCL: Serial Clock, SDA: Serial Data I/O

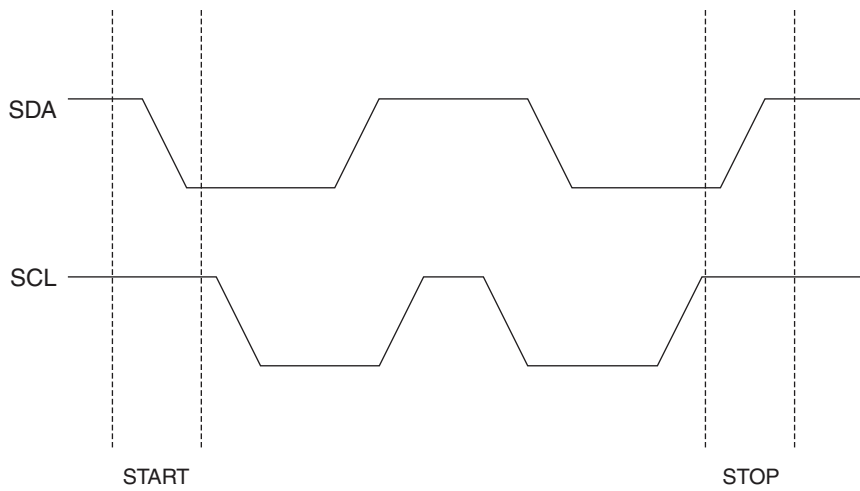


Notes: 1. The write cycle time  $t_{wr}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

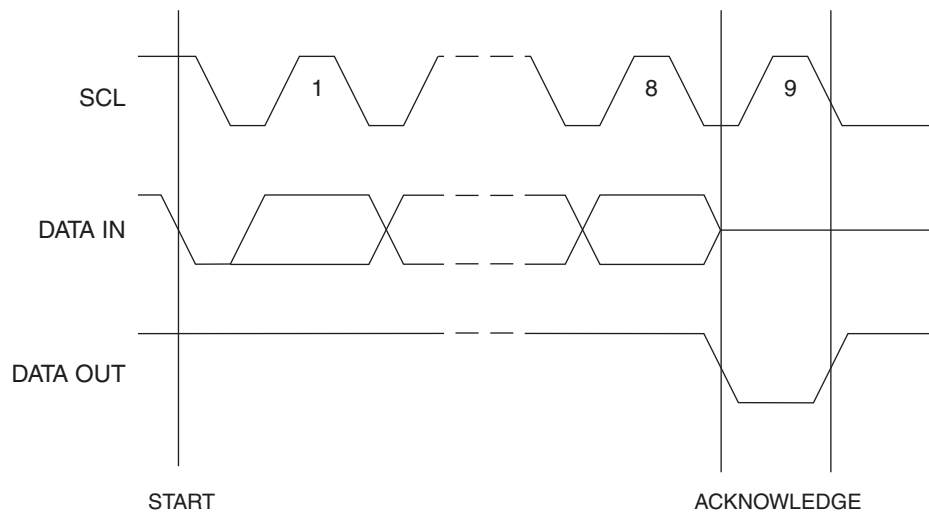
**Figure 4-4.** Data Validity



**Figure 4-5.** Start and Stop Definition



**Figure 4-6.** Output Acknowledge





## 5. Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see [Figure 7-1 on page 10](#)). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

**DATA SECURITY:** The Atmel® AT24C32D/64D has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at  $V_{CC}$ .

## 6. Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see [Figure 7-2 on page 10](#)).

**PAGE WRITE:** The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see [Figure 7-3 on page 11](#)).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

**ACKNOWLEDGE POLLING:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

## 7. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

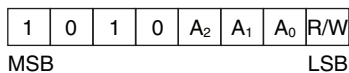
**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see [Figure 7-4 on page 11](#)).

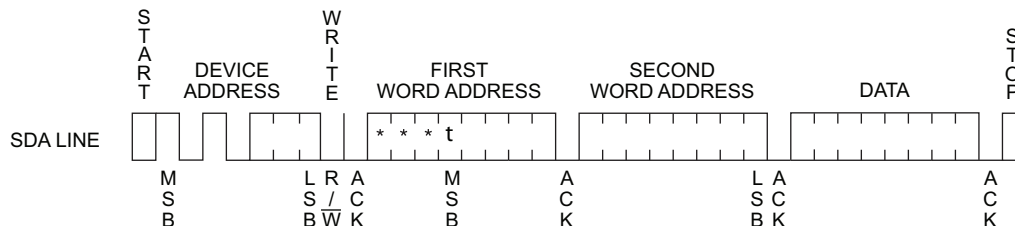
**RANDOM READ:** A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 7-5 on page 11](#)).

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 7-6 on page 11](#)).

**Figure 7-1.** Device Address

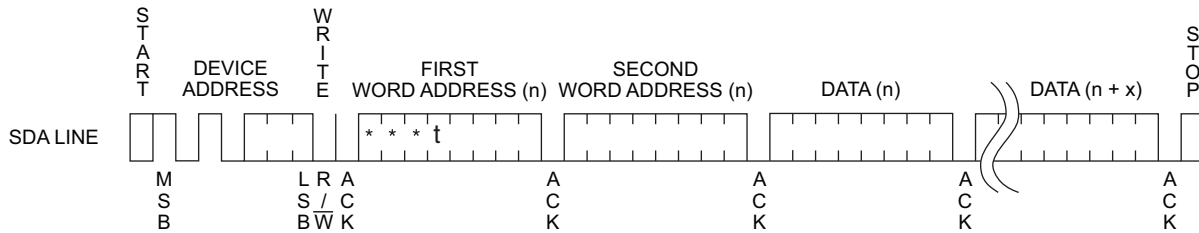


**Figure 7-2.** Byte Write



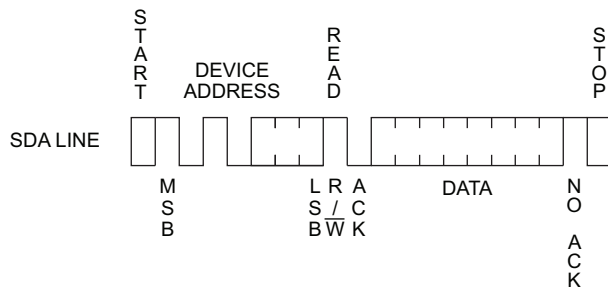
- Notes:
1. \* = DON'T CARE bits
  2. t = DON'T Care bit for Atmel AT24C32D

**Figure 7-3. Page Write**

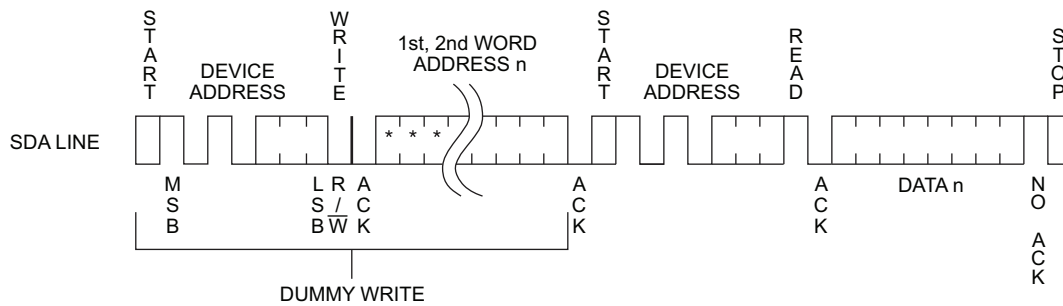


- Notes: 1. \* = DON'T CARE bits  
2. t = DON'T CARE bit for Atmel AT24C32D

**Figure 7-4. Current Address Read**

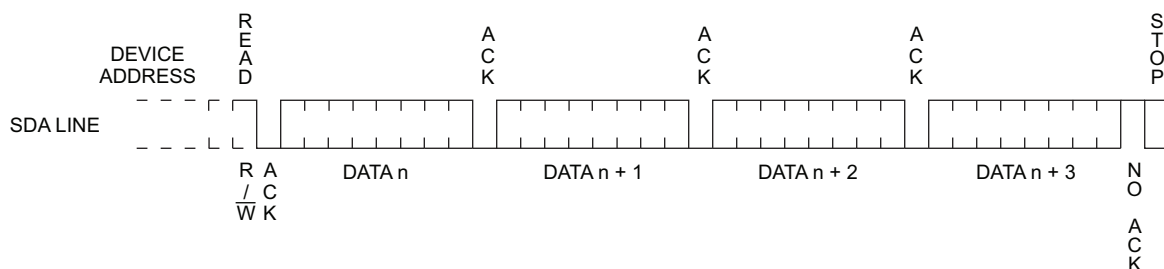


**Figure 7-5. Random Read**

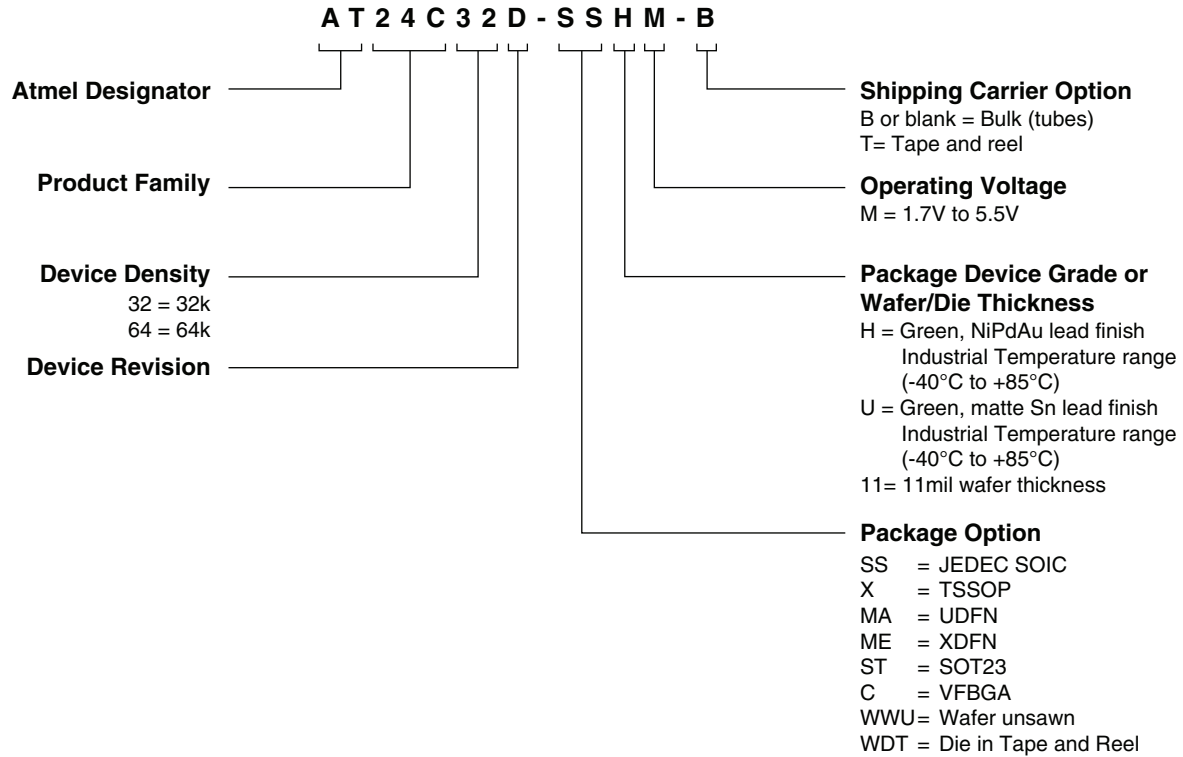


- Notes: 1. \* = DON'T CARE bits

**Figure 7-6. Sequential Read**



## 8. Ordering Code Detail



## 9. Part Markings

### 9.1 Atmel AT24C32D

#### Atmel AT24C32D-SSHM

<p>Top Mark</p> <pre>  --- --- --- --- --- --- --- ---   A  T  M  L  H  Y  W  W  --- --- --- --- --- --- --- ---   3  2  D  M                @  --- --- --- --- --- --- --- ---   *  LOT NUMBER  --- --- --- --- --- --- --- ---     PIN 1 INDICATOR (DOT) </pre>	<p>Seal Year</p> <pre>   Seal Week        --- --- ---  </pre>	<p>Y = SEAL YEAR</p> <pre> 8: 2008    2: 2012 9: 2009    3: 2013 0: 2010    4: 2014 1: 2011    5: 2015 </pre>	<p>WW = SEAL WEEK</p> <pre> 02 = Week 2 04 = Week 4 :: : :::: : 50 = Week 50 52 = Week 52 </pre>
---	---	---	--

@ = Country of Assembly

BOTTOM MARK

No Bottom Mark

#### Atmel AT24C32D-XHM

<p>Top Mark</p> <pre> PIN 1 INDICATOR (DOT)      --- --- --- --- --- ---   *  A  T  H  Y  W  W   --- --- --- --- --- ---     3  2  D  M                @   --- --- --- --- --- ---     ATMEL LOT NUMBER   --- --- --- --- --- ---  </pre>	<p>Y = SEAL YEAR</p> <pre> 8: 2008    2: 2012 9: 2009    3: 2013 0: 2010    4: 2014 1: 2011    5: 2015 </pre>	<p>WW = SEAL WEEK</p> <pre> 02 = Week 2 04 = Week 4 :: : :::: : 50 = Week 50 52 = Week 52 </pre>
---	---	--

@ = Country of Assembly

No Bottom Mark

#### Atmel AT24C32D-MAHM

<p>Top Mark</p> <pre>  --- --- ---   3  2  D  --- --- ---   H  M  @  --- --- ---   Y  T  C  --- --- ---   *    PIN 1 INDICATOR (DOT) </pre>	<p>Y = YEAR OF ASSEMBLY</p> <p>TC= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK)</p> <p>Y = SEAL YEAR</p> <pre> 8: 2008    2: 2012 9: 2009    3: 2013 0: 2010    4: 2014 1: 2011    5: 2015 </pre>
---	---



## 9.2 Atmel AT24C64D

### Atmel AT24C64D-SSHM

Top Mark	Seal Year	Y = SEAL YEAR	WW = SEAL WEEK
	Seal Week	8: 2008	02 = Week 2
		9: 2009	03 = Week 3
--- --- --- --- --- --- ---		0: 2010	04 = Week 4
A T M L H Y W W		1: 2011	05 = Week 5
--- --- --- --- --- --- ---			50 = Week 50
6 4 D M @			52 = Week 52
--- --- --- --- --- --- ---		@ = Country of Assembly	
* LOT NUMBER			
--- --- --- --- --- --- ---			
		BOTTOM MARK	
PIN 1 INDICATOR (DOT)		No Bottom Mark	

### Atmel AT24C64D-XHM

Top Mark	Y = SEAL YEAR	WW = SEAL WEEK
PIN 1 INDICATOR (DOT)	8: 2008	02 = Week 2
	9: 2009	03 = Week 3
--- --- --- --- --- ---	0: 2010	04 = Week 4
* A T H Y W W	1: 2011	05 = Week 5
--- --- --- --- --- ---		50 = Week 50
6 4 D M @		52 = Week 52
--- --- --- --- --- ---	@ = Country of Assembly	
ATMEL LOT NUMBER		
--- --- --- --- --- ---	No Bottom Mark	

### Atmel AT24C64D-MAHM

Top Mark	Y = YEAR OF ASSEMBLY
	TC= TRACE CODE (ATEMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK)
--- --- ---	Y = SEAL YEAR
6 4 D	8: 2008
--- --- ---	9: 2009
H M @	0: 2010
--- --- ---	1: 2011
Y T C	
--- --- ---	
*	
PIN 1 INDICATOR (DOT)	





## 10. Ordering Codes

### Atmel AT24C32D Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C32D-SSHM-B <sup>(1)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free Industrial Temperature (-40°C to +85°C)
AT24C32D-SSHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT24C32D-XHM-B <sup>(1)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C32D-XHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C32D-MAHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT24C32D-MEHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT24C32D-STUM-T <sup>(2)</sup>	1.7 to 5.5	5TS1	
AT24C32D-CUM-T <sup>(2)</sup>	1.7 to 5.5	8U3-1	
AT24C32D-WWU11M <sup>(3)</sup>	1.7 to 5.5	Die Sale	Industrial Temperature (-40°C to +85°C)

- Notes:
1. "-B" denotes bulk delivery
  2. "-T" denotes tape and reel delivery. SOIC = 4K/reel. TSSOP, UDFN, XDFN, SOT23 and VFBGA = 5K/reel
  3. For Wafer sales, please contact Atmel Sales

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Dual no Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body, (XDFN)
5TS1	5-lead, 1.60mm Body, Plastic Thin Shrink Small Outline Package (SOT-23)
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)





## Atmel AT24C64D Ordering Information

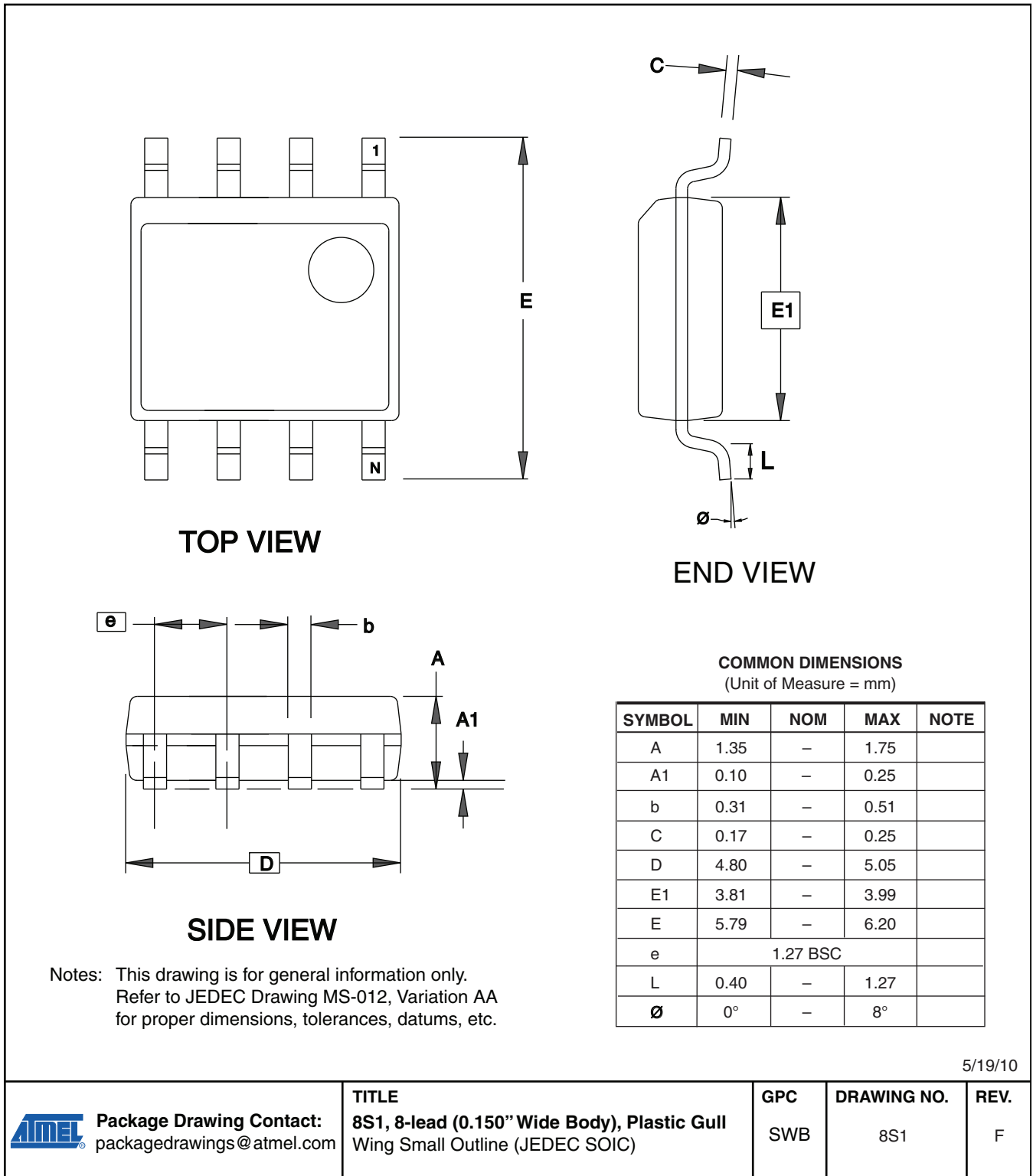
Ordering Code	Voltage	Package	Operation Range
AT24C64D-SSHM-B <sup>(1)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8S1	Lead-free/Halogen-free Industrial Temperature (-40°C to +85°C)
AT24C64D-SSHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8S1	
AT24C64D-XHM-B <sup>(1)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C64D-XHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8A2	
AT24C64D-MAHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8Y6	
AT24C64D-MEHM-T <sup>(2)</sup> (NiPdAu Lead Finish)	1.7 to 5.5	8ME1	
AT24C64D-CUM-T <sup>(2)</sup>	1.7 to 5.5	8U3-1	
AT24C64D-WWU11M <sup>(3)</sup>	1.7 to 5.5	Die Sale	Industrial Temperature (-40°C to +85°C)

- Notes: 1. "-B" denotes bulk delivery  
 2. "-T" denotes tape and reel delivery. SOIC = 4K/reel. TSSOP, UDFN, XDFN, SOT23 and VFBGA = 5K/reel  
 3. For Wafer sales, please contact Atmel Sales

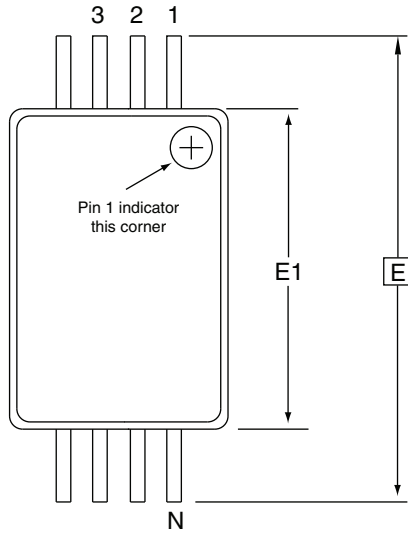
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4mm Body, Plastic, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00mm x 3.00mm Body, 0.50mm Pitch, Ultra Thin Dual no Lead Package (UDFN)
8ME1	8-lead, 1.80mm x 2.20mm Body, (XDFN)
8U3-1	8-ball, 1.50mm x 2.00mm Body, 0.50mm Pitch, Small Die Ball Grid Array (VFBGA)

11. Packaging Information

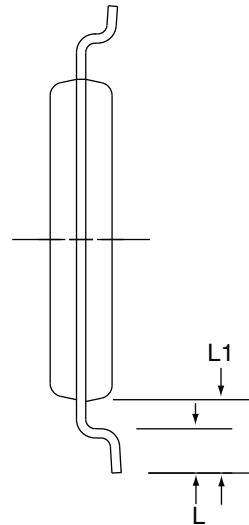
8S1 – JEDEC SOIC



## 8A2 – TSSOP



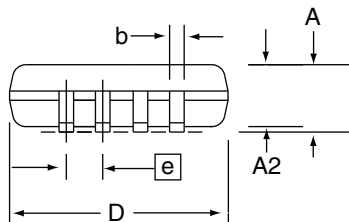
Top View



End View

### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			



Side View

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

5/19/10



Package Drawing Contact:  
packagedrawings@atmel.com

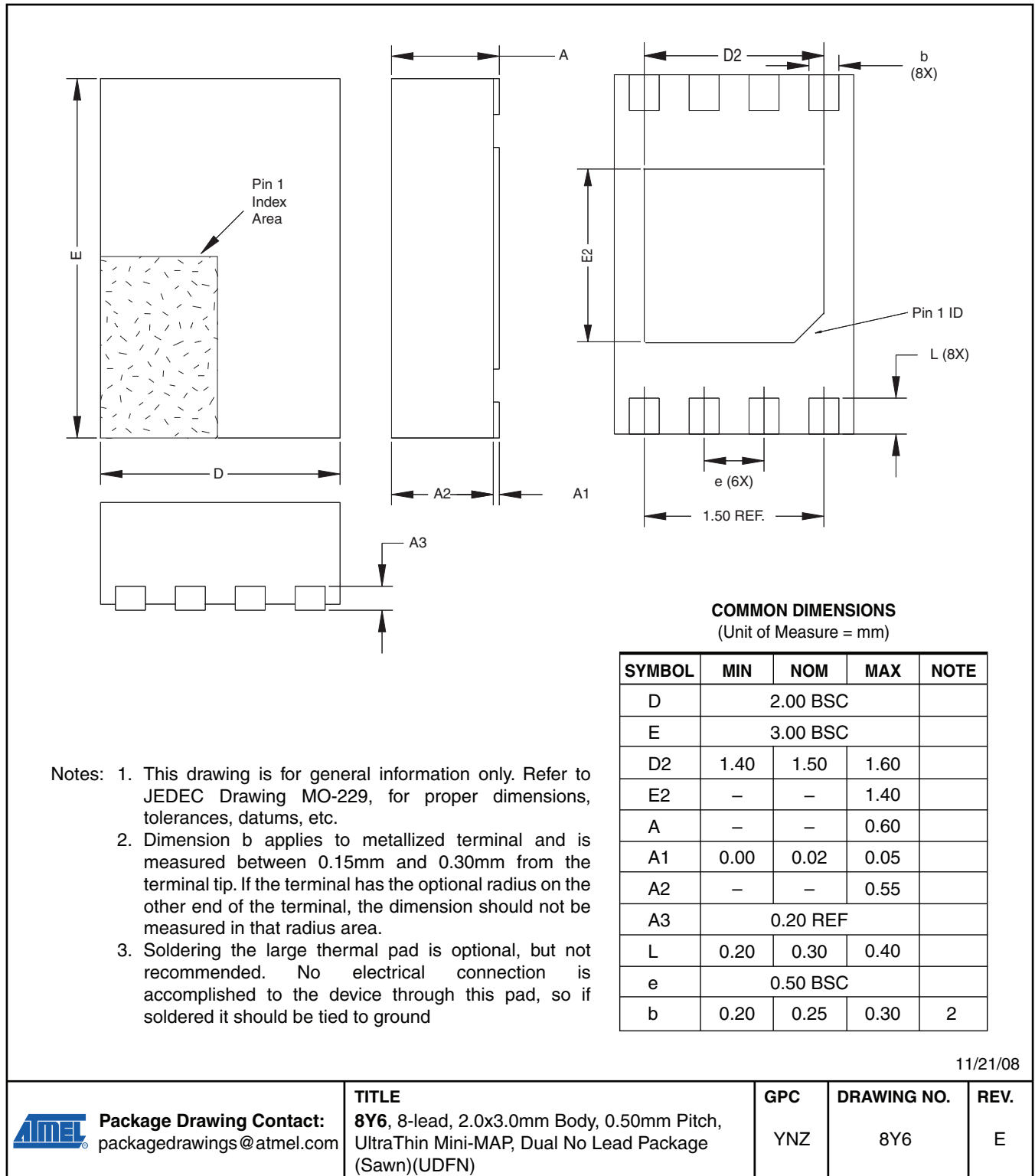
**TITLE**  
8A2, 8-lead 4.4mm Body, Plastic Thin  
Shrink Small Outline Package (TSSOP)

**GPC**  
TNR

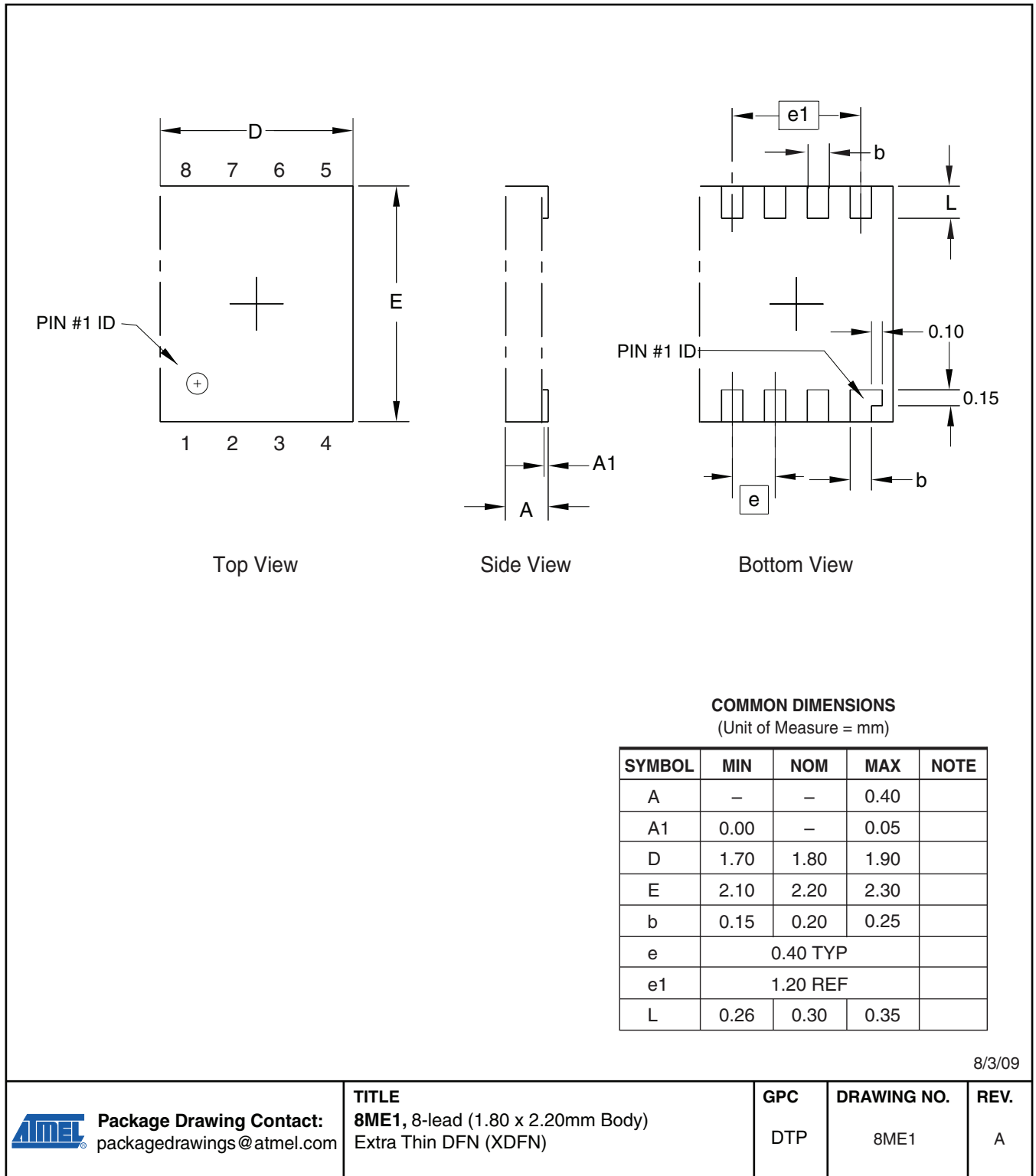
**DRAWING NO.**  
8A2

**REV.**  
E

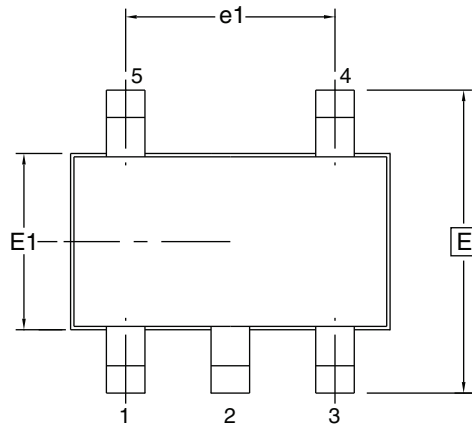
## 8Y6 – MLP



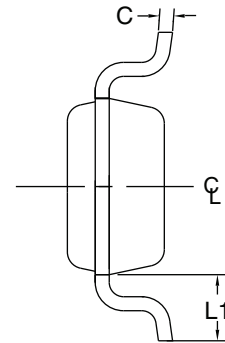
### 8ME1 – XDFN



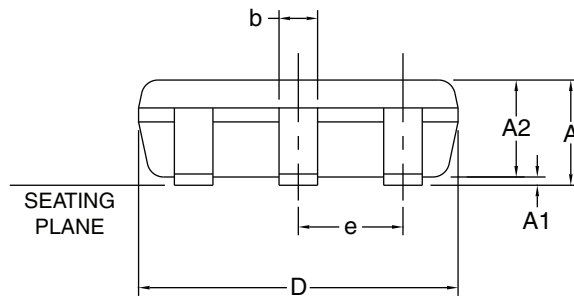
## 5TS1– SOT-23



Top View



End View



Side View

### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.10	
A1	0.00	–	0.10	
A2	0.70	0.90	1.00	
c	0.08	–	0.20	3
D	2.90 BSC			1, 2
E	2.80 BSC			1, 2
E1	1.60 BSC			1, 2
L1	0.60 REF			
e	0.95 BSC			
e1	1.90 BSC			
b	0.30	–	0.50	3, 4

- Notes:
- Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.15mm per end. Dimensions E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15mm per side.
  - The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.
  - These dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
  - Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.80mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
  - This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

11/05/08



**Package Drawing Contact:**  
packagedrawings@atmel.com

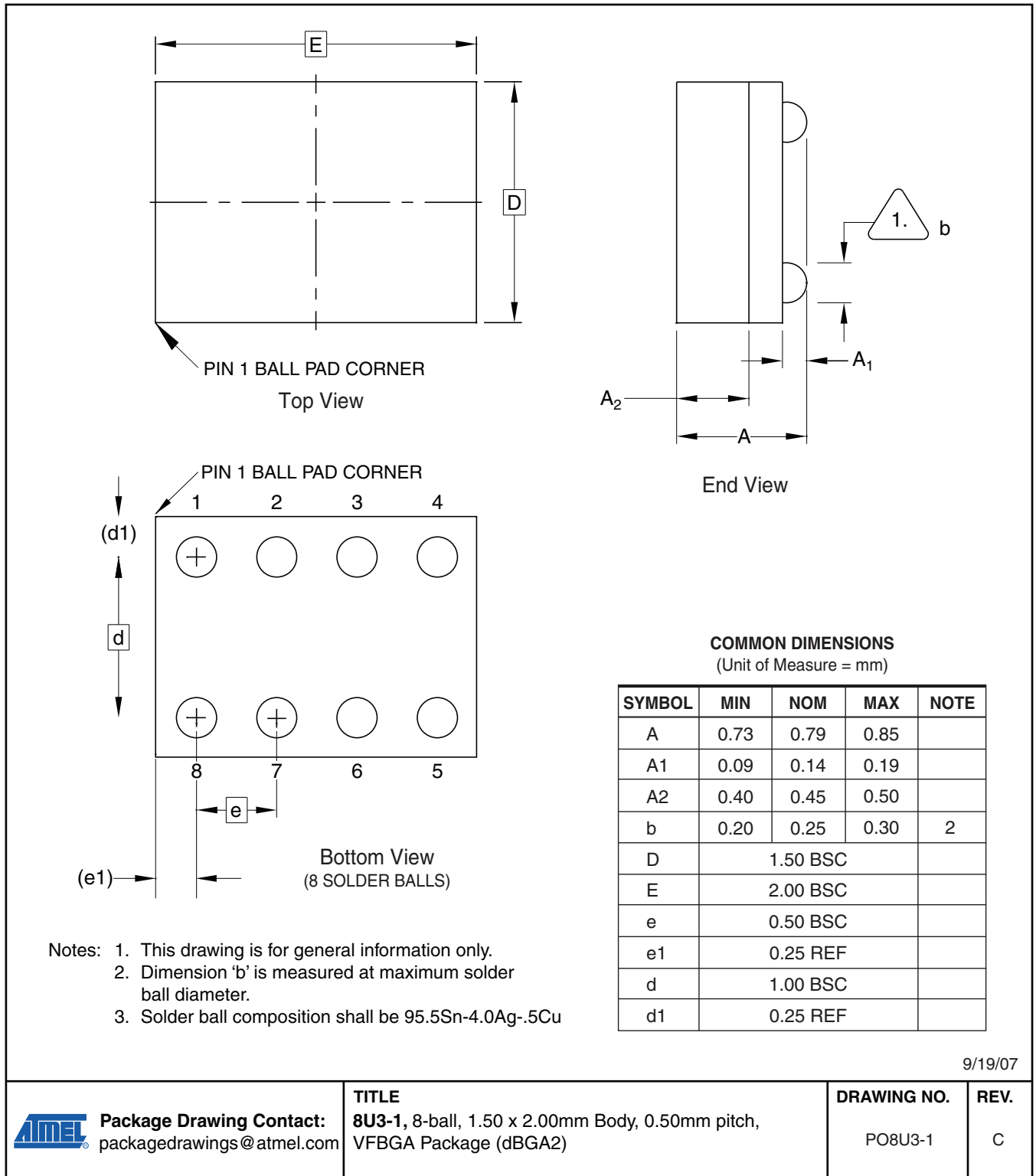
**TITLE**  
5TS1, 5-lead, 1.60mm Body, Plastic Thin  
Shrink Small Outline Package (Shrink SOT)

**GPC**  
TSZ

**DRAWING NO.**  
5TS1

**REV.**  
B

### 8U3-1 – VFBGA





**Revision History**

<b>Doc. Rev.</b>	<b>Date</b>	<b>Comments</b>
5298B	6/2010	Update 8A2 and 8S1 package drawings Remove all PDIP device package references Add SOT23 in feature and description list, pin configuration with note and package drawing
5298A	4/2010	Initial document release



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