HK32F030M Datasheet

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Preface

Purpose

This document introduces the block diagram, the memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F030M Series SOC, to help users quickly understand its features and functions.

Audience

This document is intended for:

- HK32F030M Developer
- HK32F030M Tester
- HK32F030M user

Release Notes

This document is corresponding to HK32F030M Series SOC.

Revision History

Version	Date	Description
1.0.0	2020/02/21	Initial release
1.0.1	2020/03/04	Update *Section 3.9 Low-power modes.*
1.0.2	2020/03/09	Update *Section 4.2.5 Operating current*.
1.0.3	2020/6/19	Update *Section 3.7.2 clock tree.*
1.0.4	2020/7/3	Update *Section 4.2.9 Flash memory characteristics.*
1.0.5	2020/10/12	Update *Section 3.22 ADC*.
1.0.6	2020/10/16	Update *Section 6.4 QFN20*.
1.1.0	2021/03/18	Update *Section 4.2.14 ADC characteristics.*
1.1.1	2021/06/01	Update *Section 4.2.14 ADC characteristics.*
1.2.0	2021/11/23	Update *Section 3.1 Block diagram, Section3.2.1 Flash features and Section 4.2.10 I/O port characteristics.*

Contents

1 Introduction

This document is the datasheet for HK32F030M series System-on-Chips (SOCs). HK32F030M is a family of basic microcontrollers (MCU) developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd, including:

- HK32F030MF4U6
- HK32F030MF4P6
- HK32F030MD4P6
- HK32F030MJ4M6

2 HK32F030M Overview

Based on ARM® Cortex®-M0 core, HK32F030M embeds a 16-Kbyte Flash, a 448-byte EEPROM and a 2-Kbyte SRAM. Its maximum frequency is 32 MHz.

All the pins of HK32F030M can be used as GPIOs, peripheral IOs or external interrupt inputs. In the application of pins except for power and ground pins. HK32F030M provides as many pins as possible.

HK32F030M provides several communication interfaces:

- 1 x high-speed USART (up to 4 Mbit/s)

USART supports synchronous and asynchronous communication, multi-master communication, LIN mode, Smart Card mode, and IrDA SIR CODEC (coder and decoder). RX and TX pins can be interchanged by software. In Stop mode, MCU can be woken up by receiving data.

- 1 x high-speed SPI/I2S (up to 16 Mbit/s)

SPI/I2S supports the full-duplex and the half-duplex communication with 4-bit to 16-bit data, Master/Slave mode, TI mode, NSS pulse mode, automatic CRC verification and the I2S protocol.

- 1 x high-speed I2C (up to 1 MHz)

I2C supports 1 MHz/400 kHz/100 kHz transmission rate, Master/Slave mode, multi-master mode, 7-bit/10-bit addressing mode and the SMBus protocol. In Stop mode, MCU can be woken up by receiving data.

HK32F030M embeds a 16-bit advanced PWM timer (total 4 PWM outputs, 3 of which can output complementary signals with dead time), a 32-bit general purpose PWM timer (total 4 PWM outputs) and a 16-bit basic timer (it can output interrupts at specified time).

HK32F030M integrates analog circuits: 1 x 12-bit ADC (up to 1 MSPS, 8-bit accuracy), 1 x power on reset (POR)/power down reset (PDR) circuit, and 1 x internal reference voltage (sampled by on-chip ADC).

HK32F030M supports multiple power consumption modes. In low-power mode, HK32F030M can be woken up automatically by an internal low-power timer.

HK32F030M can operate in the temperature range of -40°C to +85°C, and the supply voltage is 1.8 V to 3.6 V. It can meet the requirements of most application environments.

Because of its various peripheral interfaces, HK32F030M can be used in rich sets of application. Examples of these applications include:

- Programmable controllers, printers, and scanners
- Motor drivers and speed control
- Low-power terminals with sensor for Internet of Things
- UAV flight control, pylon control
- Toy products
- Household appliances
- Intelligent robots
- Smart watches, sports bracelets

2.1 Features

- CPU core
  - ARM® Cortex®-M0 core
  - Maximum frequency: 32 MHz
  - 24-bit SysTick timer
  - Supports interrupt vector remapping (through configuring Flash registers)

- Operating voltage range: 1.8 V to 3.6 V
- Operating temperature range: -40°C to +85°C
- Typical operating current
  - Run mode: 2.3mA@32 MHz@3.3V (71 µA/MHz)
  - Sleep mode：1.2mA@32 MHz@3.3V (37 µA/MHz), wake-up time: 21 ns
  - Deep Sleep mode：0.61mA@114 kHz@3.3V, wake-up time: 7.8 µs
  - Stop mode：30µA@3.3V, wake-up time: 10 µs (woken up by an external pin or an internal timer)
- CPU tracking and debugging
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (low-power mode simulation controlling, the debug peripheral clock controlling, and debug and track interfaces allocating)
- Memory
  - 16 Kbytes Flash (128 pages of 128 bytes; 32-bit data (read), 8-bit data(write))
  - Flash data security protection function (read or write protection can be set respectively)
  - 448 bytes EEPROM (programming time (byte): 30 µs)
  - 2 Kbytes SRAM
- Data security
  - CRC verification hardware unit
- Clock
  - External GPIO input clock: 1-32 MHz (select a pin from 4 GPIO input pins)
  - Internal high-speed clock (HSI): 32 MHz
  - Internal low-speed clock (LSI): 114 kHz
- Reset
  - External pin reset
  - POR/PDR
  - Software reset
  - Watchdog timer reset (IWDG and WWDG)
- GPIO
  - Up to 16 GPIOs (TSSOP20 package)
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up/pull-down resistors
  - Supports Open-drain outputs
  - High/low output drive capacity
- IOMUX pin functionality remapping controller
  - Small package (SON8), a pin can be remapped to multiple GPIOs or peripheral I/Os by IOMUX.
- Data communication interfaces
  - 1 x high-speed USART (up to 4 Mbit/s)
  - 1 x high-speed I2C (up to 1 MHz)
  - 1 x high-speed SPI/I2S (up to 16 Mbit/s)
- Timer and PWM generator

- 1 x 16-bit advanced PWM timer (total 4 PWM outputs, 3 of which can output complementary signals with dead time)
- 1 x 32-bit general-purpose PWM timer (total 4 PWM outputs)
- 1 x 16-bit basic timer (supports CPU interrupts)
- 1 x automatic wake-up timer, which can work in Stop mode.

- Beeper
  - 1 x beeper, which can output pluses at frequency of 1, 2, 4 or 8 kHz.
  - The beeper continues to work and trigger ADC sampling at fixed time in Stop mode.
- On-chip analog circuits
  - 1 x 12-bit ADC up to 1 MSPS (total 5 analog input channels, supports differential input pairs)
  - POR/PDR
  - 1 x 0.8 V internal reference voltage (sampled by ADC on chip)
- UID
  - 64-bit unique ID
- Reliability
  - Passed HBM4000V/CDM500V/MM200V/LU level tests.

2.2 Device overview

Table 2-1 HK32F030M series features

Features	HK32F030MJ4M6	HK32F030MD4P6	HK32F030MF4P6	HK32F030MF4U6
Operating voltage	1.8 V ~ 3.6 V			
Operating temperature	-40°C ~ +85°C			
CPU frequency	32 MHz			
SysTick	1			
Flash	16 Kbytes			
EEPROM	448 bytes			
SRAM	2 Kbytes			
CRC	1			
IWDG	1			
WWDG	1			
USART	1			
I2C	1			
SPI/I2S	1			
Advanced timer	1			
General-purpose timer	1			
Basic timer	1			
AWU timer	1			
Beeper	1			
ADC	• 1 x ADC • 3 channels	• 1 x ADC • 4 channels	• 1 x ADC • 5 channels	• 1 x ADC • 5 channels
POR/PDR	1			

Features	HK32F030MJ4M6	HK32F030MD4P6	HK32F030MF4P6	HK32F030MF4U6
Internal reference voltage	1			
64-bit UID	1			
External interrupt	6	14	16	16
GPIO	6	14	16	16
Package	SON8	TSSOP16	TSSOP20	QFN20

3 Function Description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor, which provides a MCU platform with low-cost and low-power consumption features. It delivers outstanding computational performance and an advanced system response to interrupts. With its embedded ARM Cortex-M0 core, HK32F030M family is compatible with ARM tools and software.

Take HK32F030MF4U6 for example, the block diagram of HK32F030M shows as follows:

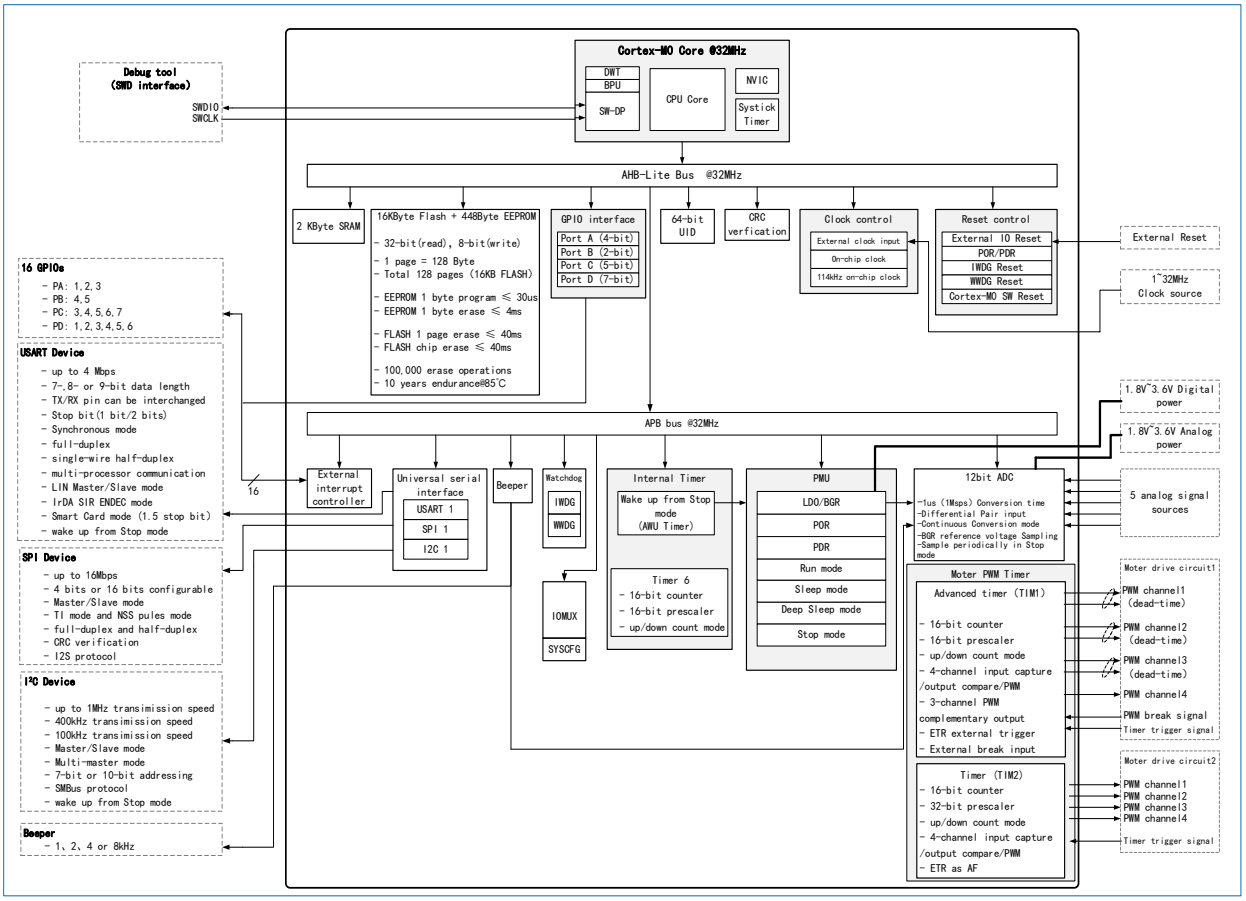

Figure 3-1 HK32F030MF4U6 MCU block diagram

3.2 Memory mapping

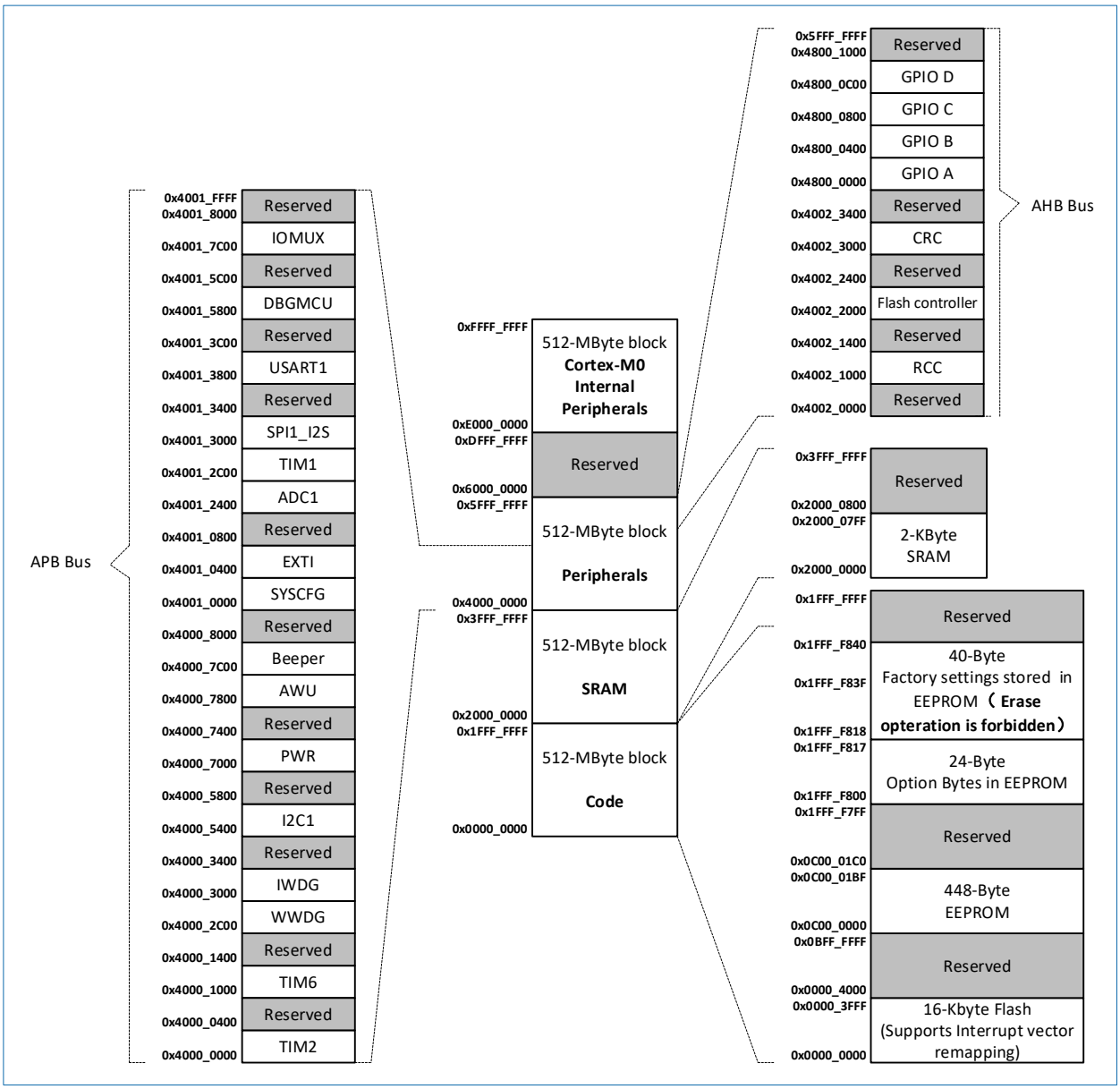

Figure 3-2 Memory mapping

3.2.1 Flash features

- Flash data width: 32 bits (read), 8 bits(write)
- 128 bytes per page
- Flash access: write in a unit of half-word (16 bit) and byte (8 bits); read in a unit of 32 bits
- Flash read/write protection
- Support interrupt vector table remapping by register configuration

Table 3-1 Flash features

Operation time	Read operation	Erase/write operation
	● Zero clock period wait, if HCLK ≤ 16 MHz ● 1 clock period wait, if 16 MHz <HCLK ≤ 32 MHz	● Write (byte): about 20 μs ● Write (half word): about 60 μs ● Flash page erase: 40 ms (Min) ● Flash mass erase: 40 ms (Min)

Endurance	Supports about 100,000 cycles erase, read and write operations.

3.2.2 Flash Option Word

Table 3-2 Flash Option Word

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF_F800	nUSER	USER	nRDP	RDP
0x1FFF_F804	nDATA1	DATA1	nDATA0	DATA0
0x1FFF_F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF_F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF_F810	IWDG_INI_KEY[15:0]		Reserved	IWDG_RL_IV[11:0]
0x1FFF_F814	DBG_CLK_CTL[15:0]		LSI_LP_CTL[15:0]	

- IWDG_RL_IV[11:0]: stores the initial value of the IWDG_RLR register. If IWDG acts as hardware watchdog, configure the IWDG_RL_IV register to set the interval of IWDG reset time.
- IWDG_INI_KEY[15:0]： to determine whether IWDG_RL_IV is valid or not. When the value of IWDG_INI_KEY equals to 0x5B1E, IWDG_RL_IV is valid, otherwise it is invalid.
- LSI_LP_CTL[15:0]： MCU enters the Stop mode after enabling IWDG, the system can be woken up by IWDG via configuring LSI_LP_CTL.
  - If LSI_LP_CTL is set to 0x369C, when MCU enters the Stop or Standby mode, LSI can be turned off according to the LSION configuration. After MCU is woken up, LSI recovers to the state before entering these modes.
  - If LSI_LP_CTL is not set, the system can be woken up by IWDG periodically after IWDG is enabled and MCU enters the Stop or Standby mode.
- DBG_CLK_CTL[15:0]: When DBG_CLK_CTL equals to 0x12DE, CPU debug clock is turned off, otherwise it stays on.

Note:

The details about the field of address 0x1FFF_F800 to 0x1FFF_F80C in Table 3-2, please refer to "Section 3.1.7: Flash option byte register" in HK32F030M Reference Manual.

3.2.3 SRAM

HK32F030M integrates a 2-Kbyte SRAM, and supports read/write access in word, half-word and byte. CPU can access SRAM fast with zero wait period to meet the requirements of most applications.

3.2.4 EEPROM

HK32F030M MCU integrates a 448-byte EEPROM.

Table 3-3 EEPROM features

Operation time	Read operation	Erase/write operation
	• Zero clock period wait, if HCLK ≤ 16 MHz • 1 clock period wait, if 16MHz <HCLK ≤ 32 MHz	• Write (byte): about 20 μs • Erase (byte): 4 ms (Min)
Endurance	Supports about 100,000 cycles erase, read and write operations; Endurance (about 10 years)	

3.3 CRC Calculation Unit

CRC is used to verify data transmission or storage integrity. HK32F030M integrates a CRC calculation unit to reduce user applications processing burden and to provide the ability to accelerate processing.

CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference

signature generated at link-time and stored at a given memory location.

3.4 NVIC

HK32F030M MCU embeds a nested vectored interrupt controller to handle interrupt flexibly with the low interrupt latency. HK32F030M has 21 external interrupt channels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Supports for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-4 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000_0000
-	-3	Fixed	Reset	Reset	0x0000_0004
-	-2	Fixed	NMI	Non-maskable interrupt	0x0000_0008
-	-1	Fixed	HardFault	All classes of fault	0x0000_000C
-	3	Settable	SVCall	System service call via SWI instruction	0x0000_002C
-	5	Settable	PendSV	Pendable request for System service	0x0000_0038
-	6	Settable	SysTick	SysTick timer	0x0000_003C
0	7	Settable	WWDG	Window Watchdog Interrupt	0x0000_0040
1	8	Settable	-	-	0x0000_0044
2	9	Settable	EXTI11	EXTI Line 11 interrupt (AWU_WKP)	0x0000_0048
3	10	Settable	Flash	Flash global interrupt	0x0000_004C
4	11	Settable	RCC	RCC global interrupt	0x0000_0050
5	12	Settable	EXTI0	EXTI Line 0 interrupt	0x0000_0054
6	13	Settable	EXTI1	EXTI Line 1 interrupt	0x0000_0058
7	14	Settable	EXTI2	EXTI Line 2 interrupt	0x0000_005C
8	15	Settable	EXTI3	EXTI Line 3 interrupt	0x0000_0060
9	16	Settable	EXTI4	EXTI Line 4 interrupt	0x0000_0064
10	17	Settable	EXTI5	EXTI Line 5 interrupt	0x0000_0068
11	18	Settable	TIM1_BRK	TIM1 break interrupt	0x0000_006C
12	19	Settable	ADC1	ADC1 interrupt (combined with EXTI line 8)	0x0000_0070
13	20	Settable	TIM1_UP_TRG_COM	TIM1 update, trigger and Com interrupts	0x0000_0074
14	21	Settable	TIM1_CC	TIM1 capture compare interrupt	0x0000_0078
15	22	Settable	TIM2	TIM2 global interrupt	0x0000_007C
16	23	Settable	-	-	0x0000_0080
17	24	Settable	TIM6	TIM6 global interrupt	0x0000_0084
18	25	Settable	-	-	0x0000_0088
19	26	Settable	-	-	0x0000_008C

Position	Priority		Name	Description	Address
20	27	Settable	-	-	0x0000_0090
21	28	Settable	EXTI6	EXTI Line 6 interrupt	0x0000_0094
22	29	Settable	EXTI7	EXTI Line 7 interrupt	0x0000_0098
23	30	Settable	I2C1	I2C global interrupt (combined with EXTI line 10)	0x0000_009C
24	31	Settable	-	-	0x0000_00A0
25	32	Settable	SPI1	SPI1 global interrupt	0x0000_00A4
26	33	Settable	-	-	0x0000_00A8
27	34	Settable	USART1	USART1 global interrupt (combined with EXTI line 9)	0x0000_00AC
28	35	Settable	-	-	0x0000_00B0
29	36	Settable	-	-	0x0000_00B4
30	37	Settable	-	-	0x0000_00B8
31	38	Settable	-	-	0x0000_00BC

3.5 EXTI

HK32F030M MCU embeds 12 external interrupt/event controller (EXTI) lines. EXTI0- EXTI7 connects to IOs, others can be configured to trigger the following events.

- EXTI8 connects to ADC to detect an AWD event
- EXTI9 connects to USART to detect a wake-up event
- EXTI10 connects to I2C to detect a wake-up event
- EXTI11 connects to automatic wake-up (AWU)events

EXTI8-EXTI10 are used as internal events, without the RTSR, FTSR, SWIE and PR register. EXTI8-EXTI10 generate ERQ and IRQ signals to wake up system by a rising edge of an event in Stop mode.

3.6 Reset

HK32F030M MCU supports System reset and Power reset.

3.6.1 System reset

Except for the reset flags in the RCC_CSR register and registers in the backup domains, System reset signal resets all the registers. When any of the following events occurs, System Reset signal is generated:

- Low level on NRST pin (External Reset)
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset): by setting SYSRESETREQ bit to ‘1’ or Cortex-M0 interrupt to perform Software reset.
- Low-power consumption management reset

You can identify a reset source by checking reset state flags in the RCC_CSR register.

3.6.2 Power Reset

When the following event occurs, Power reset signal is generated:

- POR/PDR
- Return from Standby mode

Power reset signal resets all registers except for registers in the backup domain. The reset source effects on Reset pin, and keeps low level in the progress of Reset. Reset entry vector is fixed on address 0x0000_0004.

An Internal Reset signal outputs on the NRST pin. A Pulse generator ensures that each reset source produces at least 40 us pulse latency. When NRST pin is pulled down and a reset pulse is generated for an external reset.

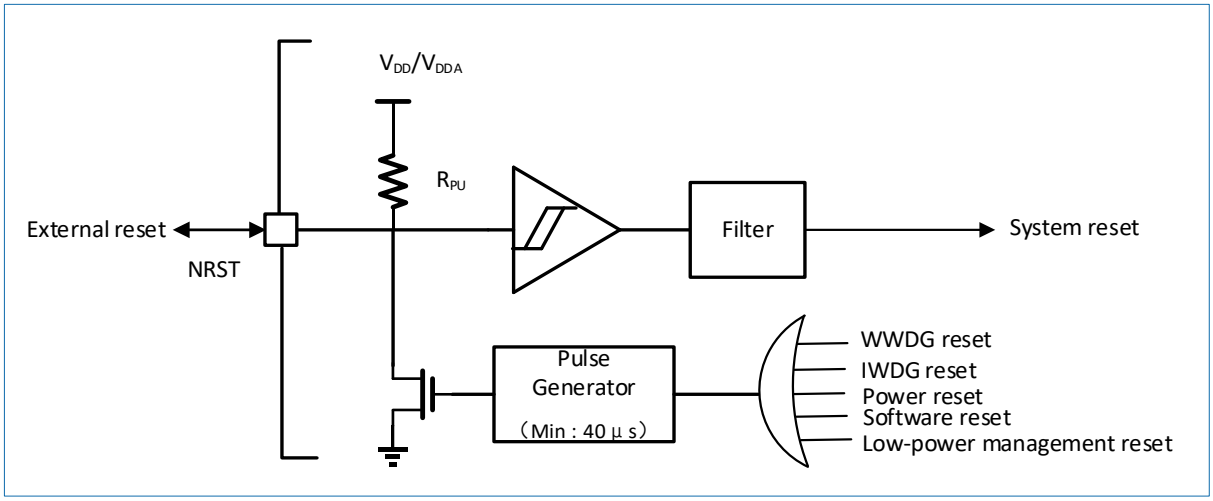

Figure 3-3 System reset

HK32F030M MCU embeds POR/PDR circuits. The circuits always operate to ensure the system runs well when power supply is over 1.8 V. When V_{DD} is less than the POR/PDR threshold, MCU resets and no external reset circuit is required.

3.7 Clock

HK32F030M selects a system clock when it starts. When it resets, 32MHz HSI RC is selected by default, and divides AHB clock frequency by 6 (5.3 MHz) as CPU clock.

HK32F030M also provides LSI or a GPIO input as a clock source for the low-power and low-cost design scheme.

3.7.1 Clock source

Table 3-5 clock sources

HSI oscillator	● Frequency: 32 MHz ● Accuracy: full temperature range ± 1%
LSI clock	● Frequency: 114 kHz ● Accuracy: full temperature range ± 4%
GPIO input clock	PA1/PD7/PB5/PC5 (up to 32 MHz)

3.7.2 Clock tree

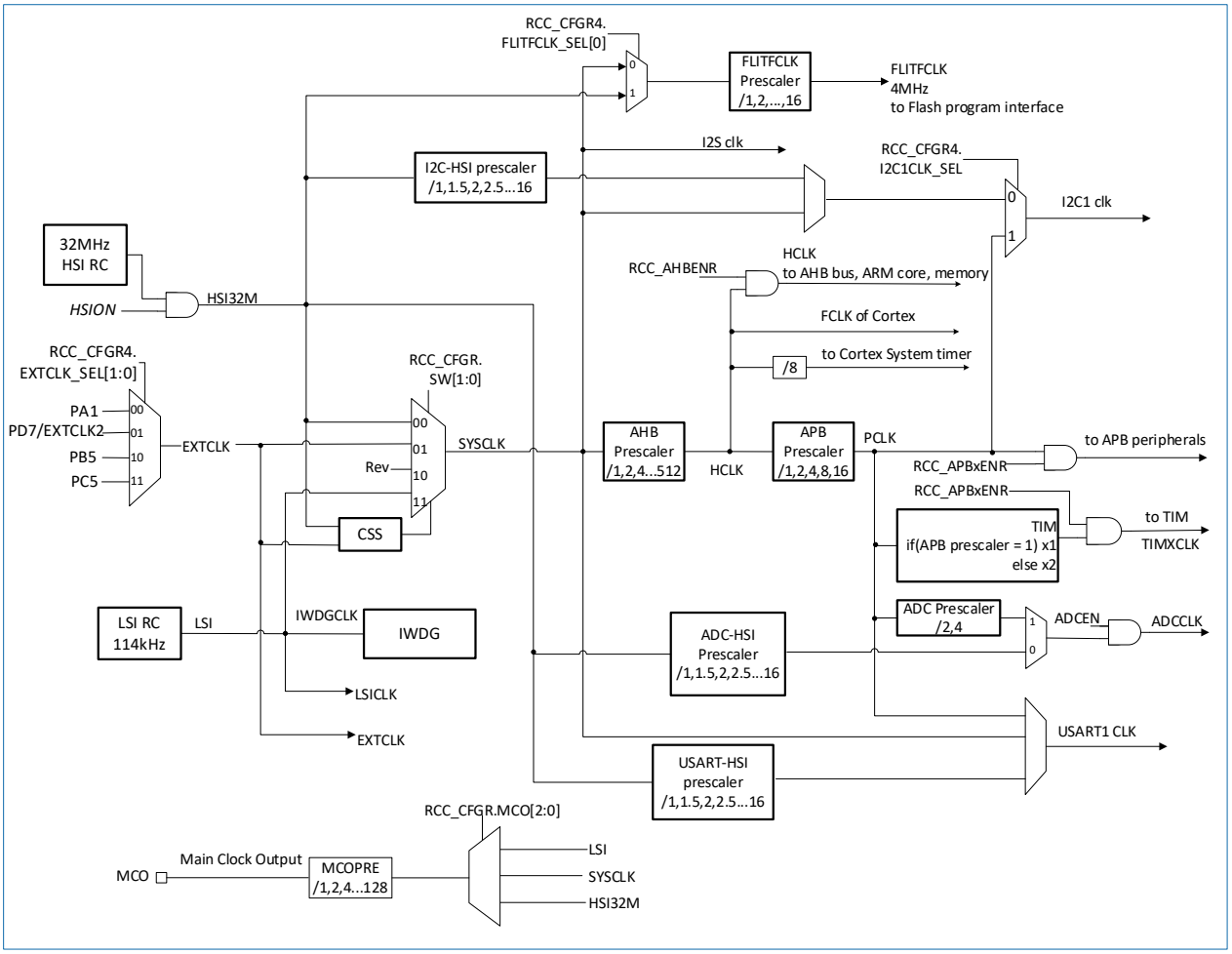

Figure 3-4 clock tree

- SYSCLK：chosen from HSI32M, LSI or GPIO. HSI32M is chosen by default.
- HCLK：AHB prescaler is set to 6 by default.
- FLITFCLK：HSI32M or SYSCLK clock
- The frequency threshold of GPIO input clock for CSS detection is adjustable.

3.8 Power Supply schemes

HK32F030M adopts a single power supply, V_{DD} and V_{DDA} multiplex the same pin to supply power for digital and analog circuits. V_{DD} and V_{DDA} is in the range of 1.8 to 3.6 V.

3.9 Low-power modes

HK32F030M supports several low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Deep Sleep mode

In Deep Sleep mode, system clock reduces to 114 kHz for saving power. In this mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. The power consumption in Deep Sleep mode is higher than that in Stop mode.

- Stop mode

Stop mode achieves the lowest power consumption while retaining the content SRAM and registers. In Stop mode, all internal clocks and HSI oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be any one of external I/O pins.

Table 3-6 operation modes and power consumption

Operation mode	Power consumption	Wake-up time
Run mode	Dynamic power consumption: 2.3mA@32MHz@3.3V(71μA/MHz)	-
Sleep mode	Dynamic power consumption: 1.2mA@32MHz@3.3V(37μA/MHz)	21 ns
Deep Sleep mode	Static power consumption: 0.61mA@32MHz@3.3	7.8 μs (Min)
Stop mode	Static power consumption: 30 μA @3.3V	10 μs

Table 3-7 shows the conditions of entering and exiting low-power modes.

Table 3-7 conditions of entering and exiting low-power modes

Operation mode	Entering the low-power mode	Wake-up condition
Sleep mode	To set: 1. PWR_CR: LPDS = 0. 2. Perform WFI/WFE command by software.	Any IRQ interrupt/event, including SysTick timer.
Deep Sleep mode	To set: 1. Switch the system clock to LSI. 2. PWR_CR: LPDS = 0. 3. Perform WFI/WFE command by software.	Any IRQ interrupt/event, including SysTick timer.
Stop mode	To set: 1. PWR_CR:LPDS = 1; 2. Set the SLEEPDEEP bit in the Cortex-M0 system control register. 3. Perform WFI/WFE command by software.	● Any EXTI line ● Supports ADC sampling driven by the beeper while MCU is pre-woken up. Really wake-up occurs when the conditions are met. ● AWU timer

3.10 Independent Watchdog

Independent watchdog (IWDG) is clocked from an internal independent 114 kHz RC. The IWDG is based on a 12-bit down counter and an 8-bit prescaler. Because it is independently from the main clock, IWDG can operate in Stop mode and Standby mode. It can be used as a watchdog to reset the system when a problem occurs or as a free running timer for application timeout management. IWDG can be configured to a software or hardware watchdog through Option bytes. In debug mode, the counter can be frozen.

3.11 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

3.12 SysTick Timer

SysTick timer is dedicated to the operation system as a standard down counter. It features:

- 24-bit down counter
- Auto-reload capability
- Generate a maskable interrupt when the counter reaches 0.

- Programmable clock source

3.13 Basic Timer

HK32F030M integrates a basic timer (TIM6).

Basic timer embeds a 16-bit counter and a 16-bit prescaler. It supports up, down, and up/down counting. Basic timer is used to generate a CPU interrupt request at fixed time. In debug mode, the counter can be frozen.

3.14 General-purpose Timer

HK32F030M integrates a synchronous 4-channel general-purpose timer (TIM2).

General-purpose timer is used to generate a PWM output or as a simple time base. TIM2 is based on a 16-bit auto-reload up/down counter and a 32-bit prescaler. In debug mode, the counter can be frozen.

TIM2 can corporate with advanced timers through Timer Linking feature for synchronization and event chaining. TIM2 is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

3.15 Advanced Timer

HK32F030M integrates an advanced timer (TIM1).

The advanced timer can be seen as a three-phase PWM on 6 channels, and used as a complete general-purpose timer. The 4 independent channels can used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, TIM1 has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer. The advanced timer can work together with general-purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

3.16 AWU Timer

HK32F030M integrates an automatic wake-up timer (AWU). The AWU timer can count and generate an interrupt to wake up MCU in Stop mode. The AWU timer embeds an ultra-low power 22-bit timer. Its operation clock can be configured to 1 to 32MHz HSE or 114 kHz LSI. The AWU timer counts down.

3.17 Beeper

The beeper embeds an ultra-low power 7-bit timer. The clock of the timer can be configured to HSE from 1 to 32 MHz or 114 kHz LSI. The counter counts down and outputs pulses at frequency of 1, 2, 4 or 8 kHz.

In Stop mode, the beeper continues to work and triggers ADC sampling at fixed time. The frequency for triggering ADC sampling is dividing the frequency of the beeper by 1024. For example, if the beeper outputs 1 kHz pulses, the frequency for triggering ADC sampling is 1 kHz/1024 ≈ 0.98 Hz (the period is about 1.02 s).

3.18 I2C Bus

A I2C bus interface can work as a master or as a slave and supports standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing mode. It supports double-slave address addressing in 7-bit slave mode. The I2C interface embeds a hardware CRC generator/checker, and supports SMBus V2.0/PMBus.

3.19 USART

HK32F030M embeds a universal synchronous/asynchronous receiver transmitter (USART1). The interface is able to communication at speeds of up to 4 Mbit/s.

The USART supports multi-processor communication, master synchronous communication and single-wire half-duplex communication.

The USART interface provides Smart Card mode (ISO 7816 compliant), IrDA SIR ENDEC support, and have LIN Master/Slave capability and automatic Baud rate detection.

The USART interface can use a clock domain independent from CPU clock to wake up MCU in Stop mode.

Table 3-8 USART1 features

features	USART1
Hardware flow control	No
DMA continuous transmission	No
Multi-processor communication	Yes
Synchronous mode	Yes
Smart Card mode	Yes
Single-wire half-duplex communication	Yes
IrDA SIR ENDEC	Yes
LIN Master/Slave mode	Yes
Dual clock domain and wake up from Stop mode	Yes
Receiver timeout	Yes
ModBus communication	Yes
Auto-baudrate detection	Yes
Driver enable	Yes

3.20 SPI

HK32F030M has a SPI interface, up to 16 Mbit/s communication speed and supports Master/Slave mode, full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies. Each frame can be configured to 4 bits or 16 bits.

The standard I2S interface (multiplexed with SPI) supports 4 different audio standards and master/slave half-duplex communication mode. The I2S interface can be configured to 16/24/32 bits transmission and operates with 16/32 bits resolution. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When operating in master mode, the I2S interface can output the master clock to external DAC/CODEC at 256 times the sampling frequency.

Table 3-9 SPI features

Features	SPI
Hardware CRC computation	Yes
RX/TX FIFO	Yes
NSS pules mode	Yes
I2S mode	Yes
TI mode	Yes

3.21 GPIO

Each of the GPIO pins can be configured by software as output (push- pull or open-drain), as input (with or

without pull-up or pull-down) or as peripheral alternate functional. Most of GPIO pins are shared with digital or analog alternate functional. All GPIOs are high current capable. The I/Os alternate function configuration can be locked in order to avoid spurious writing to the I/O registers.

3.22 ADC

Embedded ADC module is compatible with the ADC module on HK32F03x series. But there are some differences between them. The following features belong to HK32F030M:

- There are 6 channels in total. AIN0 to AIN4 are external channels for connecting to I/Os, AIN5 is an internal channel for connecting to the internal reference voltage.
- Supports differential input mode. AIN0 and AIN1, AIN2 and AIN3 consist of two pairs of differential inputs (When ADC is configured to differential mode, the ADC channel of AIN4 and internal sampling BGR voltage is disabled).
- Only supports 12-bit ADC sampling resolution.

3.22.1 ADC External trigger source

Table 3-10 ADC external trigger sources

Name	Source	External trigger selection mode (EXTSEL[2:0])
TRG0	TIM1_TRGO	000
TRG1	TIM1_CC4	001
TRG2	TIM2_TRGO	010
TRG3	TIM6_TRGO	011
TRG4	TIM1_CC1	100
TRG5	TIM1_CC2	101
TRG6	TIM1_CC3	110
TRG7	IO_TRIG	111

IO_TRIG can be triggered by any IO. You need to configure the MODER and AFR registers corresponding to the IO. Please refer to “Section 3.5 GPIO Registers” in HK32F030M Reference Manual for details.

3.22.2 AWD wake-up function

In Stop mode, system times by the beeper and sends a signal to ADC; ADC samples the signal to wake up the ADC clock. The ADC clock gets ready to trigger ADC conversions and generates an AWD event according to ADC conversion results. An AWD event is sent to an EXTI line to wake up the system.

When applying this function, you need to configure the ADC_CR2.WAKE_EN register (including the time controller in the beeper and the ADC wake-up enable register), as well as AWD related thresholds and channels.

3.23 64-bit UID

A 64-bit unique identification (UID) provides a reference number corresponding to each HK32F030M SOC. In any circumstance, the ID is unique. You are prohibited to modify the UID. According to different applications, the 64-bit UID can be read in a unit of byte (8 bits), half-word (16 bits) or word (32 bits). The 64-bit UID is fit for the following applications:

- Used as a part number (for example, as a USB character list number or other terminal applications)
- Used as a keyword. When programming the Flash, use the UID with software encryption and decryption algorithm to improve security of the code in the Flash.
- To activate the boot process of the security mechanism.

3.24 Debug Interface

Build-in ARM SWJ-DP interface, which combined with a single wire debug interface, to realize the connection between serial single wire debug interfaces (SWDIO and SWCLK).

4 Electrical characteristics

4.1 Absolute maximum values

Note：

- *Stresses above the absolute maximum rating listed in Table 4-1 and Table 4-18 may cause permanent damage to the device.*
- *Exposure to maximum permitted conditions for extended periods may affect device reliability.*

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.5	4.0	V
V_{IN}	Input voltage on pins	V_{SS} - 0.3	V_{DD} + 4.0	
$\|\Delta V_{DDx}\|$	Variation between different V_{DD} Power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variation between different V_{DD} ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	150	mA
I_{VSS}	Total current out of Vss ground lines (sink) (1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injected current on pins (3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) (4)	±25	

(1). All main power (V_{DD}, V_{DDA}) and Ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2). Negative injected current disturbs the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.

(4). When several I/Os are submitted to a current injection, the maximum $\sum_{IINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2 Operation conditions

4.2.1 General operation conditions

Table 4-4 General operation conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	32	MHz
f_{PCLK}	Internal APB clock frequency	0	32	
V_{DD}/V_{DDA}	Standard operating voltage / Analog operating voltage (1)	1.8	3.6	V
T	operating temperature	-40	85	℃

(1). All main power (V_{DD} and V_{DDA}) pins must always be connected to the external power supply. It is recommended to add a filter capacitor.

4.2.2 Reset detection

Table 4-5 Reset detection

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_{delay}	rstn build-up time	-	-	40		μs
$V_{Threshold}$	Reset threshold	-	-	1.75		V

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge (2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset temporization	-	1.50	2.50	4.50	ms

(1) PDR circuit monitors V_{DD} and V_{DDA}, POR circuit monitors only V_{DD}.

(2) Product tested values is less than the minimum $V_{POR/PDR}$ value.

(3) Guaranteed by design, not tested in production.

4.2.4 Embedded reference voltage

Table 4-7 Embedded reference voltage

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 ~ 85°C	TBD	0.8	TBD	V

4.2.5 Operating current

Table 4-8 Operating current characteristics

Mode	Conditions	VDD=3.3V			Unit
		-40° C	25° C	85° C	
Run mode	HCLK = HSI (32 MHz), 1 wait period for Flash read operation. APB clock is enabled.	2.572	2.599	2.704	mA
	HCLK = HSI (32 MHz), 1 wait period for Flash read operation. APB	2.326	2.338	2.501	mA

Mode	Conditions	VDD=3.3V			Unit
		-40° C	25° C	85° C	
	clock is disabled.				
	HCLK =LSI (114 kHz)	1.802	1.711	1.822	mA
Sleep mode	HCLK = HSI (32 MHz), APB clock is disabled.	1.097	1.197	1.477	mA
Deep Sleep mode	HCLK = HSI (32 MHz), APB clock is disabled.	0.548	0.613	0.728	mA
Stop mode	Low-power state (supports automatic wake-up and LDO)	21.83	34.08	213.6	μA
	Low-power state (supports LDO)	18.02	30.12	210.44	μA

4.2.6 High-speed internal (HSI) RC oscillator

Table 4-9 HSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	32	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(HSI)}$	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register	-	-	1	
		Factory calibrated: T_A= –40 ~ +85°C	-1	-	1	%
$T_{su(HSI)}$	HSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100	μA

4.2.7 Low-speed internal (LSI) RC oscillator

Table 4-10 LSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	114	-	kHz
$DuCy_{(LSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(LSI)}$	Accuracy of the LSI oscillator	Factory setting: T_A= –40 ~+85 °C	1.5	-	2.2	
$T_{su(LSI)}$	LSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	80	100	μA

4.2.8 GPIO input clock

HK32F030M is clocked from PA1/PD7/PB5/PC5 input clock.

Table 4-11 GPIO input clock characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
F_{ext}	Input clock frequency	1	8.0	32	MHz
	Input clock duty	40	-	60	%
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.9 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{PROG}	A byte programming time	-	30	-	μs
T_{ERASE}	Page erase time	30	40	50	ms
	Mass erase time	30	40	50	ms
I_{DDPROG}	A byte programming current	-	-	5	mA
$I_{DDERASE}$	Page/mass erase time	-	-	2	mA
I_{DDREAD}	Supply current@24MHz (read mode)	-	2	3	mA
	Supply current@1MHz (read mode)	-	0.25	0.4	mA
N_{END}	Endurance	100			kcycles
t_{RET}	Data retention	10			year

4.2.10 I/O port characteristics

Table 4-13 I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	VDD = 3.3 V	1.65@without Schmitt 1.75@with Schmitt			V
V_{IL}	Input low level voltage		-0.3		1.60@ with Schmitt 1.45@ without Schmitt	V
V_{hys}	Schmitt trigger voltage hysteresis		450mV@3.3V	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 3.3 V	-	-	3	μA
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	30	40	50	KΩ
R_{PD}	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}$	30	40	50	KΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

4.2.11 Output voltage characteristics

Table 4-14 Output voltage characteristics

Symbol	Description	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	V_{DD}=3.3V I_{OL}=-8mA	0	0.8	V
V_{OH}	Output high level voltage	V_{DD}=3.3V I_{OH}=8mA	2.4	3.3	
V_{OL}	Output low level voltage	V_{DD}=3.3V I_{OL}=-20mA	0	0.8	
V_{OH}	Output high level voltage	V_{DD}=3.3V I_{OH}=20mA	2.4	3.3	

Table 4-15 Output voltage AC characteristics

Mode	Symbol	Description	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 2V ~	-	2	MHz

Mode	Symbol	Description	Conditions	Min	Max	Unit
	$t_{f(IO)out}$	Output high to low level fall time	3.6V	-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 2 V ~ 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, VDD = 2.7 V ~ 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, VDD = 2.7 V ~ 3.6 V	-	5	ns
	$t_{r(IO)out}$	Output low to high level rise time	CL = 50 pF, VDD = 2.7 V ~ 3.6 V	-	5	ns

4.2.12 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit might connect to an external RC circuit or no circuit.

Table 4-16 NRST pin characteristics

Symbol	Description	Min	Max	Unit
V_{IL}	NRST input low level voltage		0.8	V
V_{IH}	NRST input high level voltage	2		V
V_{hys}	Schmitt trigger voltage hysteresis		200	mV
R_{pull}	Weak pull-up equivalent resistor		50	K
T_{Noise}	Low level is neglected		100	ns

4.2.13 TIM timer characteristics

Table 4-17 TIM characteristics

Symbol	Description	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz
Res $_{TIM}$	Timer resolution	-	16	bit
Tcounter	16-bit counter clock period when selecting an internal clock	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536x65536	$T_{TIMxCLK}$

(1). $f_{TIMxCLK}$ = 32 MHz

4.2.14 ADC characteristics

Table 4-18 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	ADC power supply	-	2	3.3	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05		1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-		17	$1/f_{ADC}$

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{AIN}	Conversion voltage range	-	0	-	V_{DD}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-			1	kΩ
C_{ADC}	Internal sample and hold capacitor	-			5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			μs
		-	8.3			$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	μs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling rate	f_{ADC} = 14 MHz	0.107		17.1	μs
		-	1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	0	0	1	μs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
		-	14 to 252 (ts for sampling +12.5 for successive approximation)			$1/f_{ADC}$
ADC 位数	12-bit (8 bits in valid)	-	-			-

5 Typical circuitry

5.1 Power supply scheme

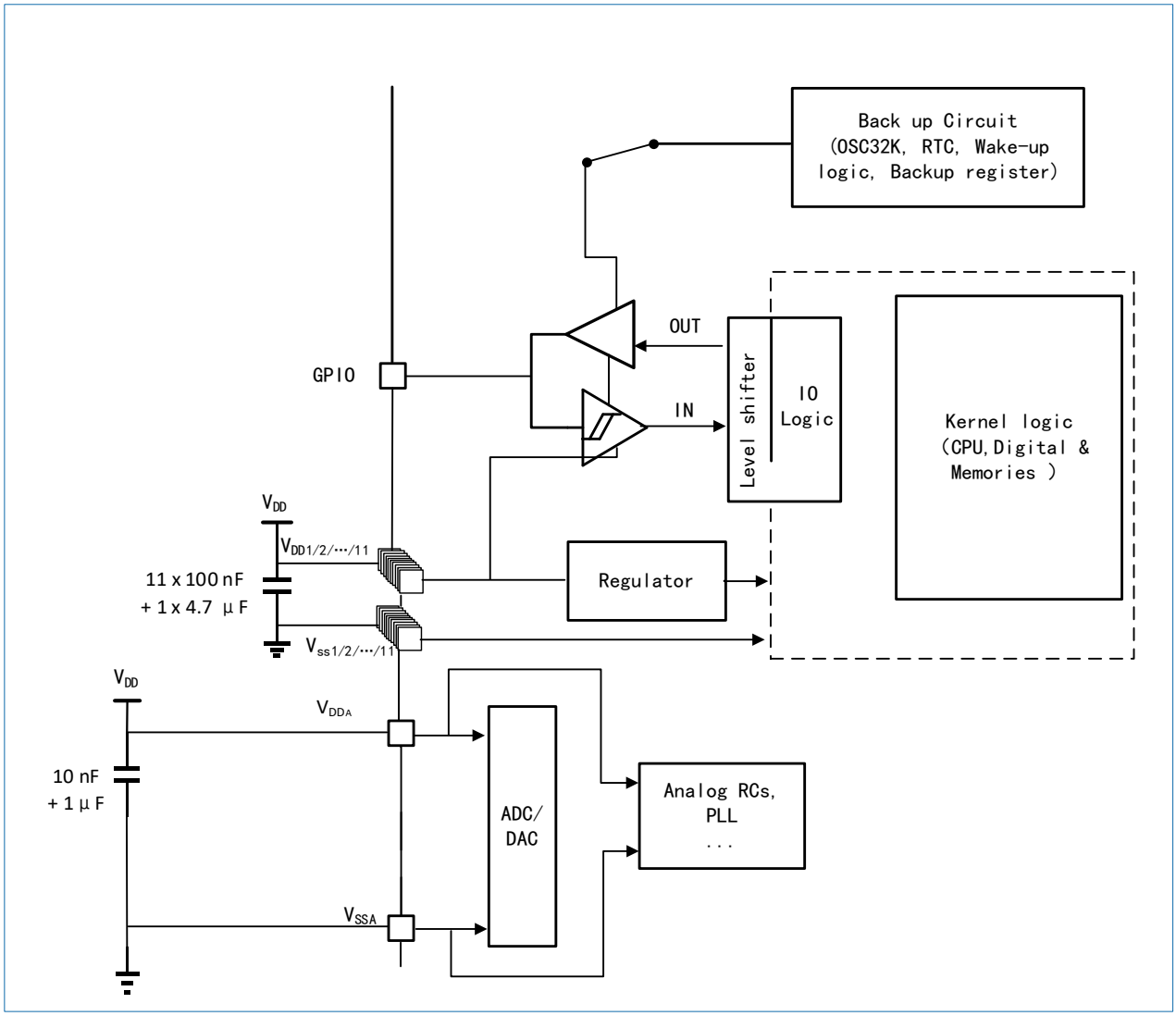

Figure 5-1 Power Supply scheme

6 Pinouts and pin descriptions

HF32F030M is available in four packages: SON8, TSSOP16, TSSOP20, and QFN20.

6.1 SON8

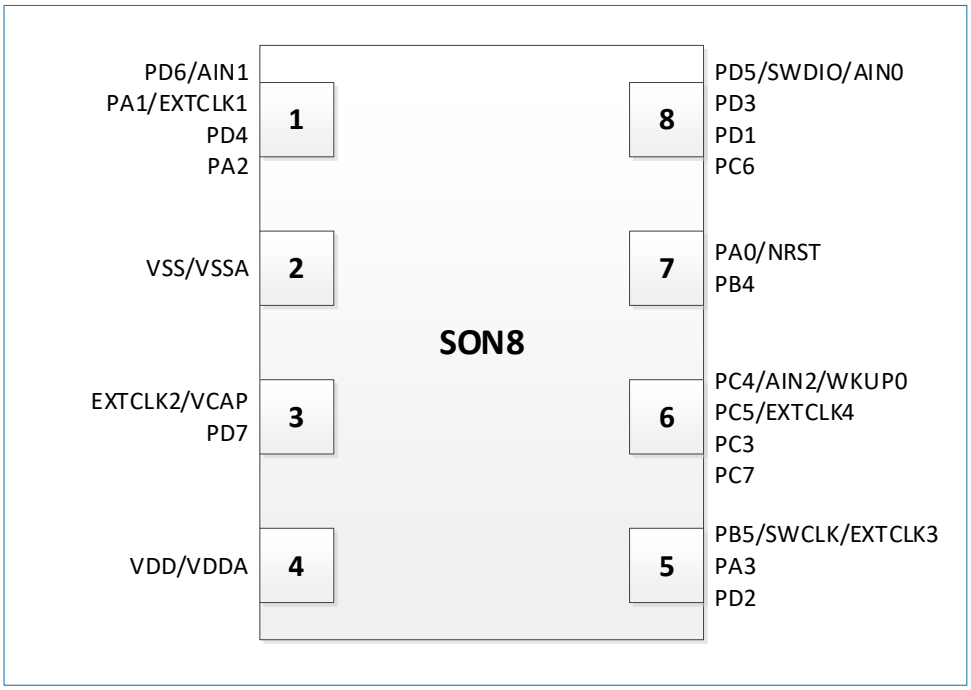

Figure 6-1 SON8 (HK32F030MJ4M6) package pinout

Table 6-1 shows pin description of SON8 package.

Table 6-1 SON8 pin descriptions

Pin #	Pin Name	Pin Type [1]	Pin Function	
			Default Function	Alternate functions
1	PD6/AIN1 [2]	I/O	PD6 GPIO	-
	PA1/HSECLK1	I/O	PA1	-
	PD4	I/O	PD4 GPIO	I2C1_SMBA
	PA2	I/O	PA2	I2C1_SMBA
2	VSS/VSSA	Ground	The Digital ground / the analog ground	
3	VCAP/PD7/HSECLK2	I/O	PD7	I2C1_SMBA
4	VDD/VDDA	Power Supply	The Digital power supply/the analog power supply	
5	PB5/SWCLK/HSECLK3	I/O	SWCLK after reset	SWCLK_I2C1_SDA [3]
	PA3	I/O	PA3	-
	PD2	I/O	PD2	-
6	PC4/AIN2 [2]	I/O	PC4	-
	PC5/HSECLK4	I/O	PC5	I2C1_SDA
	PC3	I/O	PC3	-
	PC7	I/O	PC7	-
7	NRST/PA0	I/O	NRST	-
	PB4	I/O	PB4	I2C1_SCL
8	PD5/SWDIO/AIN0 [2]	I/O	SWDIO	SWDIO

Pin #	Pin Name	Pin Type (1)	Pin Function	
			Default Function	Alternate functions
	PD3	I/O	PD3	-
	PD1	I/O	PD1	I2C1_SMBA
	PC6	I/O	PC6	I2C1_SCL

(1). I= input, O=output, I/O= input/output, S=supply.

(2). AIN0 ~ AIN3 has the ADC analog input capability.

(3). PB5 combined with extra registers configuration to enable SWCLK or I2C1_SDA.

6.2 TSSOP16

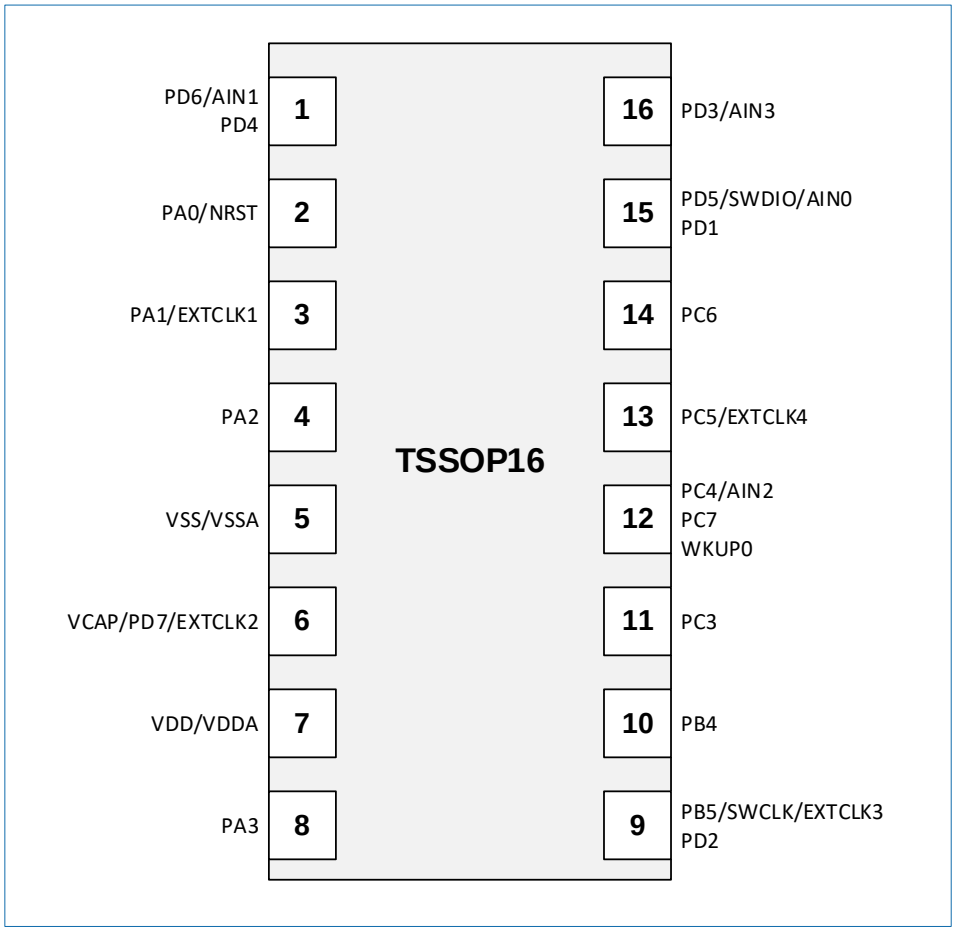

Figure 6-2 TSSOP16 (HK32F030MD4P6) package pinout

Table 6-2 shows pin description of TSSOP16 package.

Table 6-2 TSSOP16 pin descriptions

Pin #	Pin Name	Pin Type (1)	Pin Function	
			Default Function	Alternate functions
1	PD6/AIN1 (2)	I/O	PD6 GPIO	--
	PD4	I/O	PD4 GPIO	I2C1_SMBA
2	NRST/PA0	I/O	NRST	--
3	PA1/HSECLK1	I/O	PA1	--
4	PA2	I/O	PA2	I2C1_SMBA

Pin #	Pin Name	Pin Type [1]	Pin Function	
			Default Function	Alternate functions
5	VSS/VSSA	Ground	The Digital ground / the analog ground	
6	VCAP/PD7/HSECLK2	I/O	PD7	I2C1_SMBA
7	VDD/VDDA	Power Supply	The Digital power supply/the analog power supply	
8	PA3	I/O	PA3	--
9	PB5/SWCLK/HSECLK3	I/O	SWCLK after reset	SWCLK_I2C1_SDA [3]
	PD2	I/O	PD2	--
10	PB4	I/O	PB4	I2C1_SCL
11	PC3	I/O	PC3	--
12	PC4/AIN2 [2]	I/O	PC4	--
	PC7	I/O	PC7	--
13	PC5/HSECLK4	I/O	PC5	I2C1_SDA
14	PC6	I/O	PC6	I2C1_SCL
15	PD5/SWDIO/AIN0 [2]	I/O	SWDIO	SWDIO
	PD1	I/O	PD1	I2C1_SMBA
16	PD3/AIN3 [2]	I/O	PD3	--

(1). I= input, O=output, I/O= input/output, S=supply.

(2). AIN0 ~ AIN3 has the ADC analog input capability.

(3). PB5 combined with extra registers configuration to enable SWCLK or I2C1_SDA.

6.3 TSSOP20

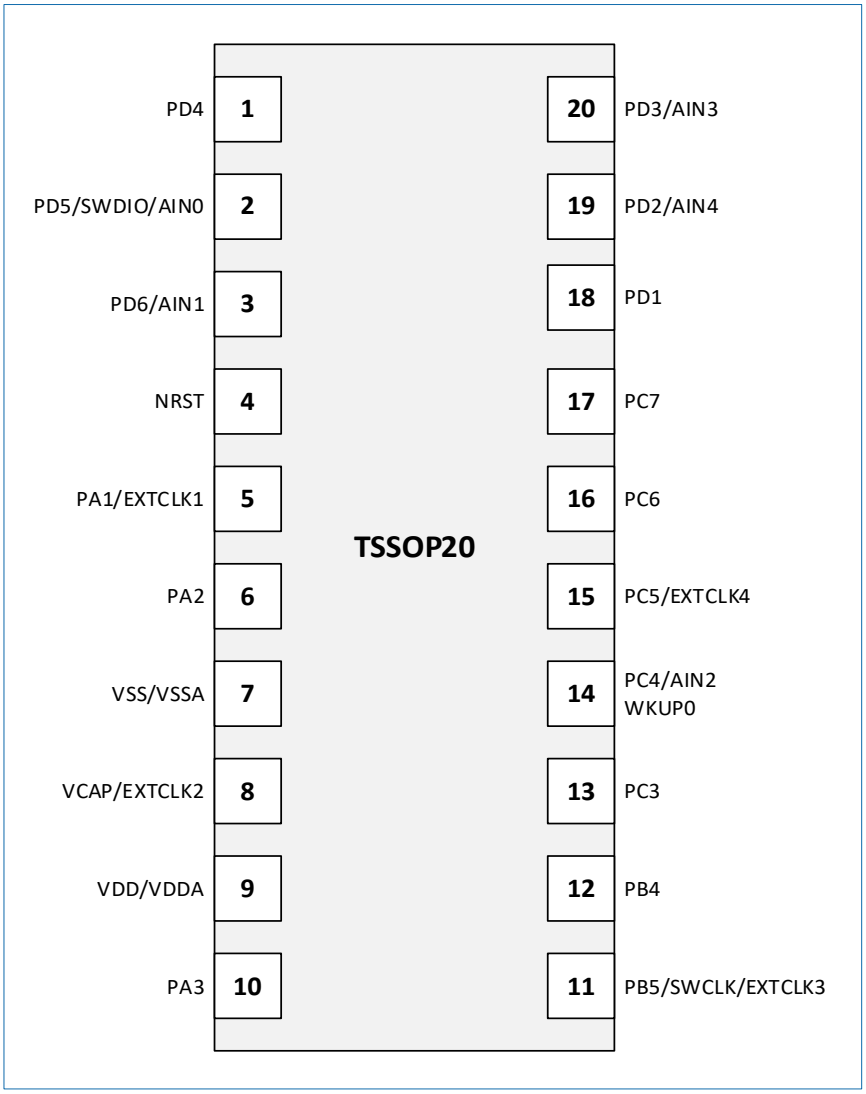

Figure 6-3 TSSOP20 (HK32F030MF4P6) package pinout

Table 6-3 shows pin description of TSSOP20 package.

Table 6-3 TSSOP20 pin descriptions

Pin #	Pin Name	Pin Type (1)	Pin Function	
			Default Function	Alternate functions
1	PD4	I/O	PD4 GPIO	I2C1_SMBA
2	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
3	PD6/AIN1	I/O	PD6 GPIO	--
4	NRST	I	NRST Input	--
5	PA1/HSECLK1	I/O	PA1	--
6	PA2	I/O	PA2	I2C1_SMBA
7	VSS/VSSA	Ground	The Digital ground / the analog ground	
8	VCAP	O	NC, Floating	
9	VDD/VDDA	Power Supply	The Digital power supply/the analog power supply	
10	PA3	I/O	PA3	--

Pin #	Pin Name	Pin Type [1]	Pin Function	
			Default Function	Alternate functions
11	PB5/SWCLK/HSECLK3	I/O	SWCLK after reset	SWCLK_I2C1_SDA[3]
12	PB4	I/O	PB4	I2C1_SCL
13	PC3	I/O	PC3	--
14	PC4/AIN2 [2]	I/O	PC4	--
15	PC5/HSECLK4	I/O	PC5	I2C1_SDA
16	PC6	I/O	PC6	I2C1_SCL
17	PC7	I/O	PC7	--
18	PD1	I/O	PD1	I2C1_SMBA
19	PD2/AIN4 [2]	I/O	PD2	--
20	PD3/AIN3 [2]	I/O	PD3	--

(1). I= input, O=output, I/O= input/output, S=supply.

(2). AIN0 ~ AIN3 has the ADC analog input capability.

(3). PB5 combined with extra registers configuration to enable SWCLK or I2C1_SDA.

6.4 QFN20

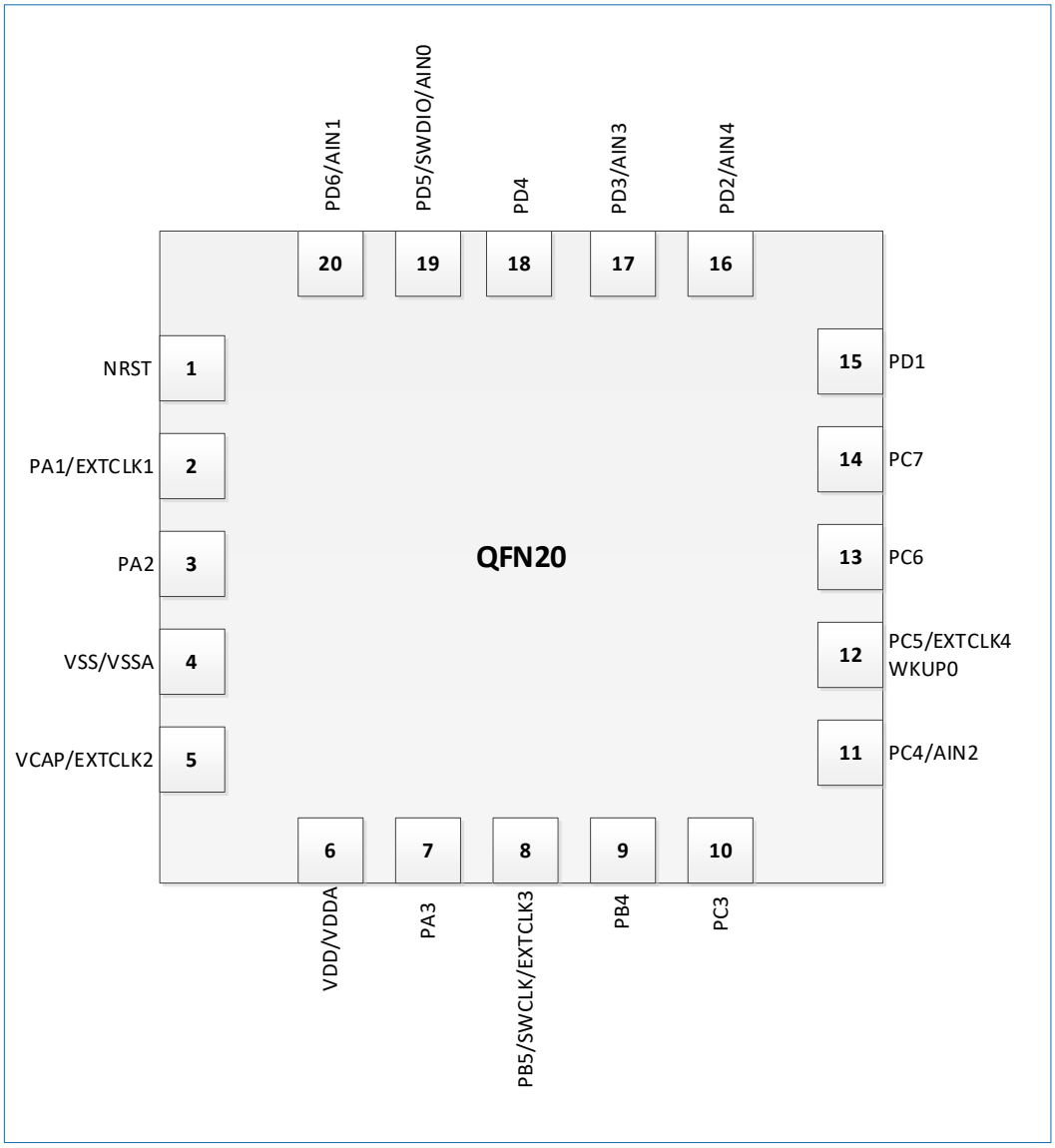

Figure 6-4 QFN20(HK32F030MF4U6) package pinout

Table 6-4 shows pin description of QFN20 package.

Table 6-4 QFN20 pin descriptions

Pin #	Pin Name	Pin Type (1)	Pin Functions	
			Default Functions	Alternate functions
1	NRST	I	NRST Input	--
2	PA1/HSECLK1	I/O	PA1	-
3	PA2	I/O	PA2	I2C1_SMBA
4	VSS/VSSA	Ground	The Digital ground / the analog ground	
5	VCAP	O	NC, Floating	
6	VDD/VDDA	Power Supply	The Digital power supply/the analog power supply	
7	PA3	I/O	PA3	-
8	PB5/SWCLK/HSECLK3	I/O	SWCLK after reset	SWCLK_I2C1_SDA (3)
9	PB4	I/O	PB4	I2C1_SCL

Pin #	Pin Name	Pin Type (1)	Pin Functions	
			Default Functions	Alternate functions
10	PC3	I/O	PC3	-
11	PC4/AIN2 (2)	I/O	PC4	-
12	PC5/HSECLK4	I/O	PC5	I2C1_SDA
13	PC6	I/O	PC6	I2C1_SCL
14	PC7	I/O	PC7	-
15	PD1	I/O	PD1	I2C1_SMBA
16	PD2/AIN4 (2)	I/O	PD2	-
17	PD3/AIN3 (2)	I/O	PD3	-
18	PD4	I/O	PD4 GPIO	I2C1_SMBA
19	PD5/SWDIO/AIN0 (2)	I/O	SWDIO	SWDIO
20	PD6/AIN1 (2)	I/O	PD6 GPIO	-

(1). I= input, O=output, I/O= input/output, S=supply.

(2). AIN0 ~ AIN3 has the ADC analog input capability.

(3). PB5 combined with extra registers configuration to enable SWCLK or I2C1_SDA.

6.5 Pin Alternate functions

Table 6-5 Pin Alternate functions

Pin Name	AF0 (I2C1/SWD)	AF1 (USART1)	AF2 (SPI1/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6(Beeper)	AF7 (ADC1)
PA0	Reserved	Reserved	Reserved	TIM1_BKIN	TIM2_CH3	RCC_MCO	BEEP	ADC1_ETR
PA1	Reserved	Reserved	Reserved	TIM1_CH1N	TIM2_ETR	RCC_MCO	BEEP	ADC1_ETR
PA2	I2C1_SMBA	Reserved	SPI1_SCK/I2S_CK	TIM1_CH2N	TIM2_CH4	RCC_MCO	BEEP	ADC1_ETR
PA3	Reserved	USART1_TX	SPI1_NSS/I2S_WS	TIM1_CH3N	TIM2_CH3	RCC_MCO	BEEP	ADC1_ETR
PB4	I2C1_SCL	USART1_RX	SPI1_MISO/I2S_MCK	TIM1_CH2N	TIM2_ETR	RCC_MCO	BEEP	ADC1_ETR
PB5	SWCLK_I2C1_SDA (1)	USART1_RX	SPI1_NSS/I2S_WS	TIM1_BKIN	TIM2_CH2	RCC_MCO	BEEP	ADC1_ETR
PC3	Reserved	USART1_CK	Reserved	TIM1_CH3_CH1N (2)	TIM2_CH1	RCC_MCO	BEEP	ADC1_ETR
PC4	Reserved	Reserved	SPI1_MISO/I2S_MCK	TIM1_CH4_CH2N (2)	TIM2_CH4	RCC_MCO	BEEP	ADC1_ETR
PC5	I2C1_SDA	Reserved	SPI1_SCK/I2S_CK	TIM1_ETR	TIM2_CH1	RCC_MCO	BEEP	ADC1_ETR
PC6	I2C1_SCL	Reserved	SPI1_MOSI/I2S_SD	TIM1_CH1	TIM2_CH3	RCC_MCO	BEEP	ADC1_ETR
PC7	Reserved	Reserved	SPI1_MISO/	TIM1_CH2	TIM2_ETR	RCC_MCO	BEEP	ADC1_ETR

Pin Name	AF0 (I2C1/SWD)	AF1 (USART1)	AF2 (SPI1/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6(Beeper)	AF7 (ADC1)
			I2S_MCK					
PD1	I2C1_SMBA	USART1_TX	Reserved	TIM1_CH1	TIM2_CH4	RCC_MCO	BEEP	ADC1_ETR
PD2	Reserved	Reserved	SPI1_MOSI/I2S_SD	TIM1_CH2	TIM2_CH3	RCC_MCO	BEEP	ADC1_ETR
PD3	Reserved	Reserved	SPI1_SCK/I2S_CK	TIM1_CH3	TIM2_CH2	RCC_MCO	BEEP	ADC1_ETR
PD4	I2C1_SMBA	USART1_CK	SPI1_MOSI/I2S_SD	TIM1_CH4	TIM2_CH1	RCC_MCO	BEEP	ADC1_ETR
PD5	SWDIO	USART1_TX	Reserved	TIM1_ETR	TIM2_ETR	RCC_MCO	BEEP	ADC1_ETR
PD6	Reserved	USART1_RX	SPI1_MISO/I2S_MCK	TIM1_CH2	TIM2_CH2	RCC_MCO	BEEP	ADC1_ETR
PD7	I2C1_SMBA	USART1_RX	SPI1_NSS/I2S_WS	TIM1_CH3	TIM2_CH1	RCC_MCO	BEEP	ADC1_ETR

(1). PB5 is combined with the following register to select SWCLK or I2C1_SDA.

(2). PC3 and PC4 are combined with the following peripheral registers to select CH3/CH4 or CH1N/CH2N of TIM1.

bit	2	1	0
	PB5_I2C1_SEL	**PC4_TIM1_SEL**	**PC3_TIM1_SEL**
access	rw	rw	rw
reset value	0	0	0

Figure 6-5 PB5/PC4/PC3 Alternate function selection

- If PB5_AF is configured to AF0, the value of PB5_I2C1_SEL is:
  - 0: PB5 is used as SWCLK input pin (the default setting when system resets).
  - 1: PB5 is used as I2C1 SDA pin.
- If PC4_AF is configured to AF3, the value of PC4_TIM1_SEL is:
  - 0: PC3 is used as TIM1 CH4 pin.
  - 1: PC3 is used as TIM1 CH2N pin.
- If PC3_AF is configured to AF3, the value of PC3_TIM1_SEL is:
  - 0: PC3 is used as TIM1 CH3 pin.
  - 1: PC3 is used as TIM1 CH1N pin.

6.6 IOMUX pin function remapping

TSSOP16/SON8 package has IOMUX pin function remapping controller. It can remap a pin to multiple GPIOs or a peripheral IO.

Take the pin 8 in Figure 6-1 for example to describe the pin remapping.

Table 6-6 Function mapping of the pin 8 in SON8 package

Operation	Function of the pin 8
Chip Reset	PD5 and the peripheral IO corresponding to the SYSCFG configuration.
Configuring IOMUX registers	● PD3 and the peripheral IO corresponding to the SYSCFG configuration. ● PD1 and the peripheral IO corresponding to the SYSCFG configuration. ● PC6 and the peripheral IO corresponding to the SYSCFG configuration.

SON8/SOP8 package can use 18 GPIOs and the IO functions of all peripheral flexibly by IOMUX configuration.

7 Package characteristics

7.1 SON8

SON8 is a 4.9 x 6 mm and 1.27 mm pitch package.

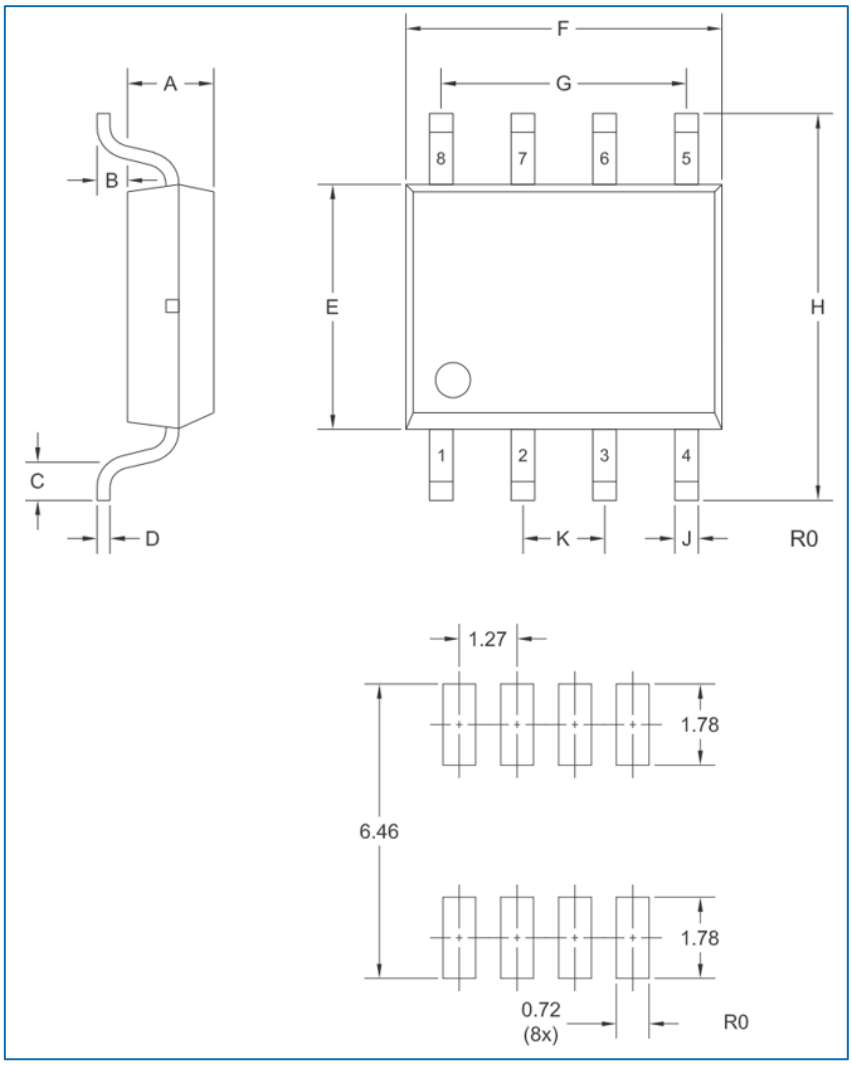

Figure 7-1 SON8 package outline

Table 7-1 SON8 package parameters

Symbol	Unit: mm		Unit: inches[1]	
	Min	Max	Min	Max
A	1.24	1.44	0.049	0.057
B	0.00	0.27	0.000	0.011
C	0.46	-	0.018	-
D	0.16	0.27	0.006	0.011
E	3.70	3.90	0.145	0.154
F	4.81	5.01	0.189	0.198
G	3.81		0.150	
H	5.88	6.18	0.231	0.244
J	0.35	0.52	0.013	0.021
K	1.27		0.050	

7.2 TSSOP16

TSSOP16 is a 5.0 mm x 4.4 mm and 0.65 mm pitch package.

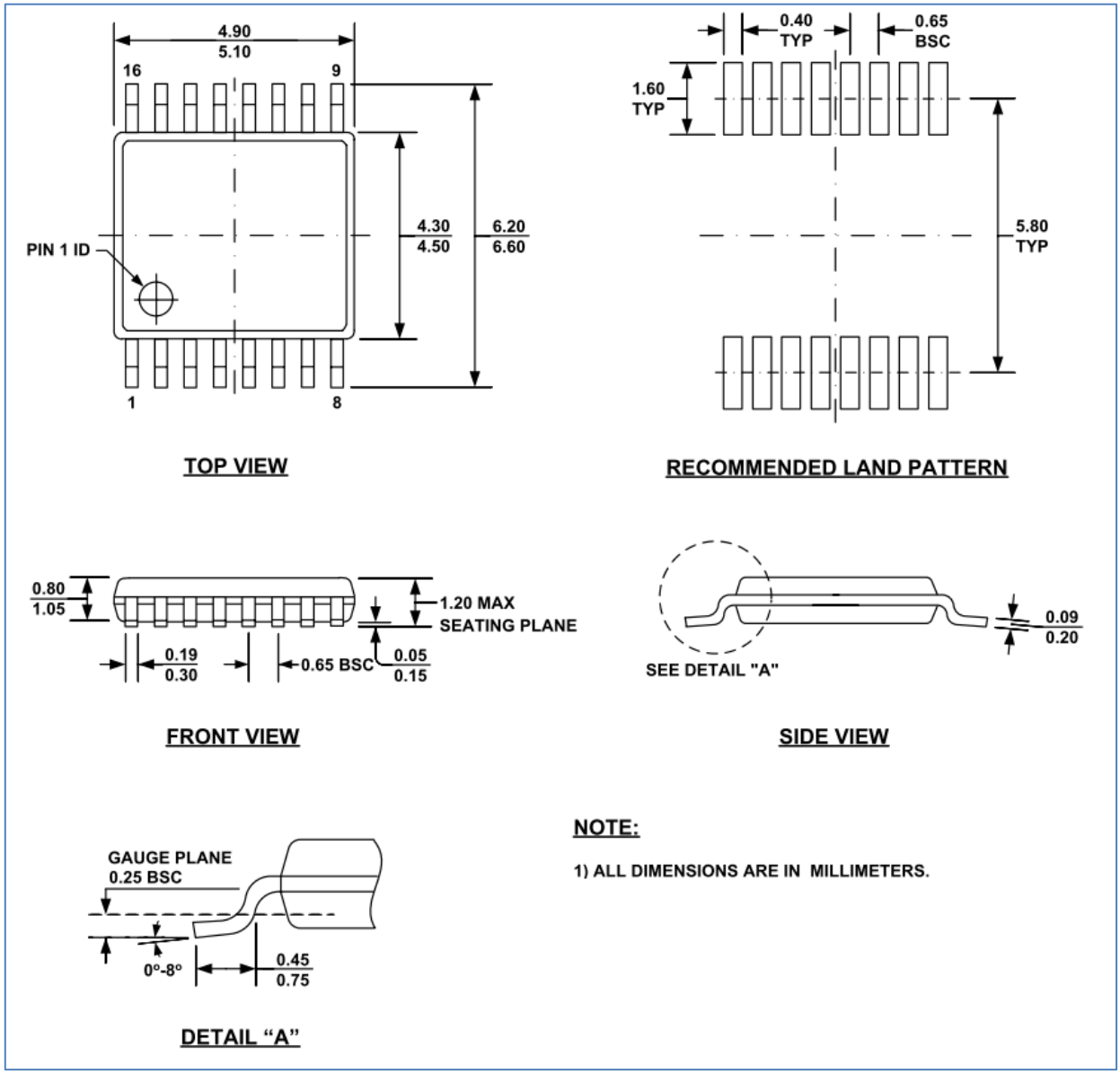

Figure 7-2 TSSOP16 package outline

7.3 TSSOP20

TSSOP20 is a 6.5 mm x 4.4 mm and 0.65 mm pitch package.

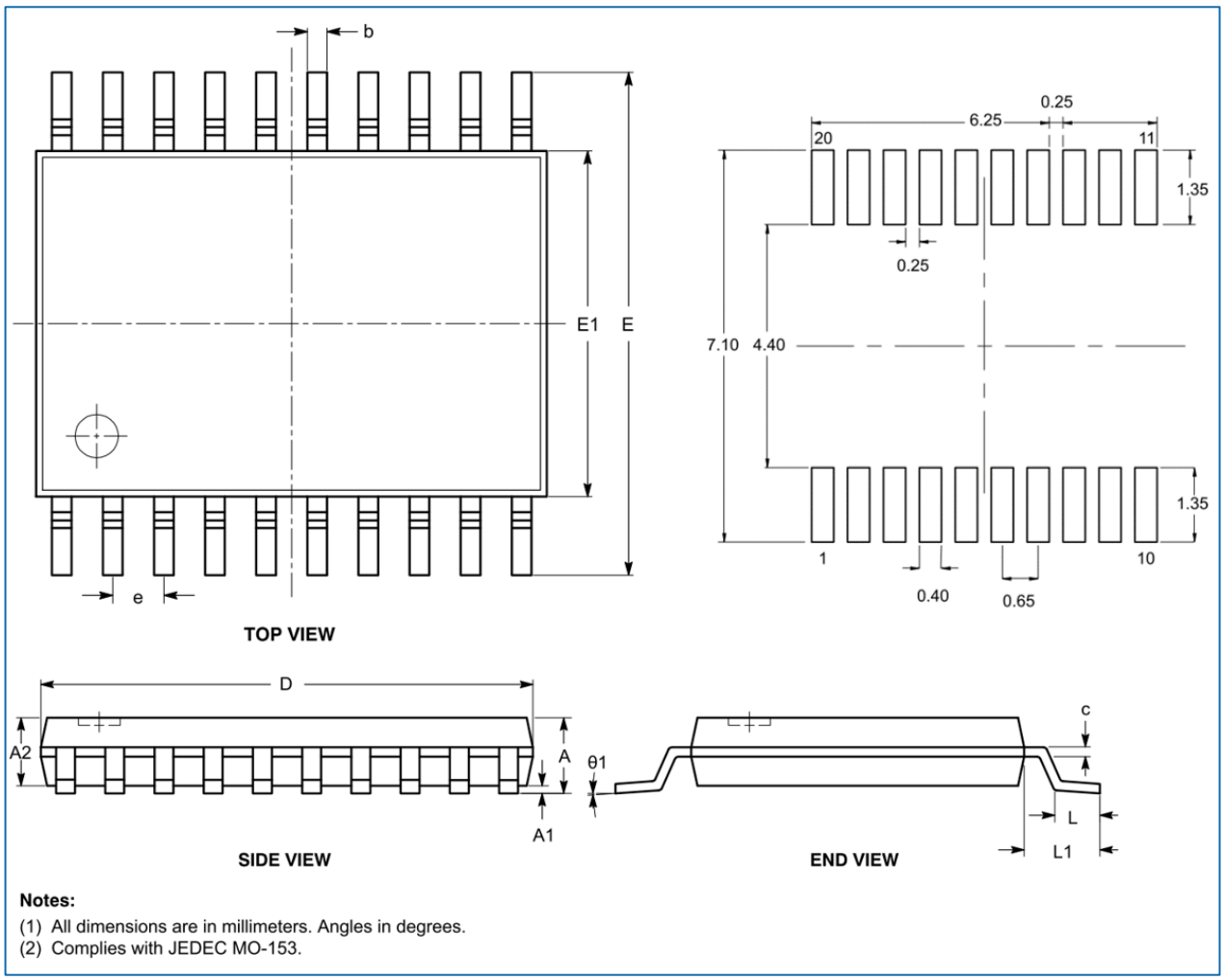

Figure 7-3 TSSOP20 package outline

Table 7-2 TSSOP20 package parameters

Symbol	Min(mm)	Typ(mm)	Max(mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°

7.4 QFN20

QFN20 is a 4 mm x 4 mm and 0.5 mm pitch package.

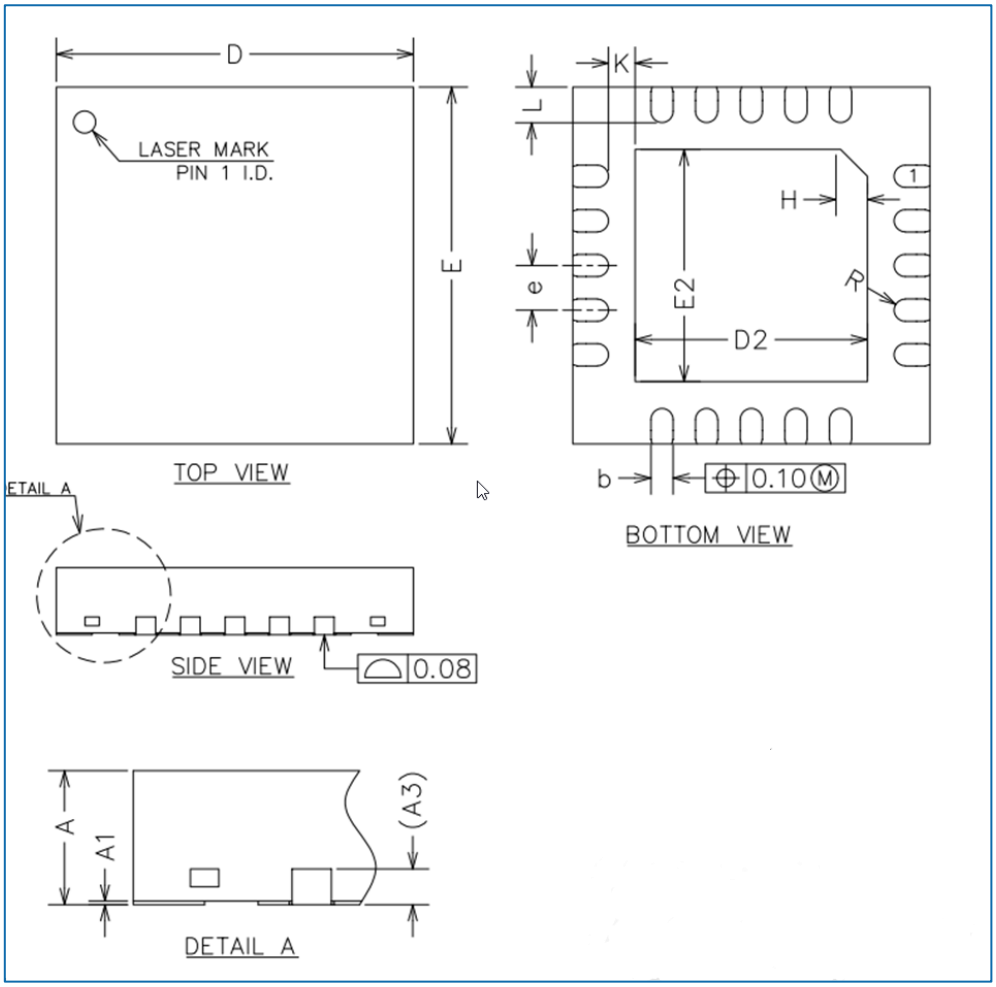

Figure 7-4 QFN20 package outline

Table 7-3 QFN20 package parameters

Symbol	Min(mm)	Typ(mm)	Max(mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
H	0.30 REF		
K	0.20	-	-
L	0.35	0.40	0.45
R	0.10	-	-

8 Ordering information

Table 8-1 HK32F030M ordering information

HK32F030M series	Packaging	Comments
HK32F030MF4U6	Tape and reel/Tray	-
HK32F030MF4P6	Tape and reel/Tube	-
HK32F030MD4P6	Tape and reel/Tube	-
HK32F030MJ4M6	Tape and reel/Tray	-

9 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EXTI	Extended Interrupts and Events Controller
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

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