19-0523; Rev 1; 2/11

EVALUATION KIT AVAILABLE

Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

MAX1436B

General Description

The MAX1436B octal, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power and high-dynamic performance in medical imaging instrumentation and digital communications applications. The MAX1436B operates from a 1.8V single supply and consumes only 743mW (93mW per channel) while delivering a 69.9dB (typ) signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1436B features a low-power standby mode for idle periods.

An internal 1.24V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range. The reference architecture is optimized for low noise.

A single-ended clock controls the data-conversion process. An internal duty-cycle equalizer compensates for wide variations in clock duty cycle. An on-chip PLL generates the high-speed serial low-voltage differential signal (LVDS) clock.

The MAX1436B has self-aligned serial LVDS outputs for data, clock, and frame-alignment signals. The output data is presented in two's complement or binary format.

The MAX1436B offers a maximum sample rate of 40Msps. See the *Pin-Compatible Versions* table below for higher-speed versions. This device is available in a small, 14mm x 14mm x 1mm, 100-pin TQFP package with exposed pad and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

Ultrasound and Medical Imaging

Instrumentation

Multichannel Communications

Features

- **Excellent Dynamic Performance**
  - **69.9dB SNR at 5.3MHz**
  - **96dBc SFDR at 5.3MHz**
  - **95dB Channel Isolation**
- **Ultra-Low Power**
  - **93mW per Channel (Normal Operation)**
  - **Fast 200μs Wake-Up Time from Standby**
- **Serial LVDS Outputs**
- **Pin-Selectable LVDS/SLVS (Scalable Low-Voltage Signal) Mode**
- **LVDS Outputs Support Up to 30 Inches FR-4 Backplane Connections**
- **Test Mode for Digital Signal Integrity**
- **Fully Differential Analog Inputs**
- **Wide Differential Input Voltage Range (1.4V_{P-P})**
- **On-Chip 1.24V Precision Bandgap Reference**
- **Clock Duty-Cycle Equalizer**
- **Compact, 100-Pin TQFP Package with Exposed Pad**
- **Evaluation Kit Available (Order MAX1436BEVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1436BECQ+D	-40°C to +85°C	100 TQFP-EP* (14mm x 14mm x 1mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.
D = Dry pack.
**EP = Exposed pad.*

Pin-Compatible Versions

PART	SAMPLING RATE (Msps)	RESOLUTION (Bits)	POWER-SAVE MODE
MAX1434	50	10	Power-down
MAX1436	40	12	Power-down
MAX1436B	40	12	Standby
MAX1437	50	12	Power-down
MAX1438	65	12	Power-down

Pin Configuration appears at the end of data sheet.

Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
AVDD..-0.3V to +2.0V
CVDD..-0.3V to +3.6V
OVDD ....-0.3V to +2.0V
IN_P, IN_N ....-0.3V to (V_{AVDD} + 0.3V)
CLK ....-0.3V to (V_{CVDD} + 0.3V)
OUT_P, OUT_N, FRAME_, CLKOUT_......-0.3V to (V_{OVDD} + 0.3V)
DT, SLVS/$\overline{LVDS}$, LVDSTEST, PLL_, $\overline{T}$/B, STBY,
REFIO, REFADJ, CMOUT..................-0.3V to (V_{AVDD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 47.6mW/°C above +70°C)...............3809.5mW
Operating Temperature Range ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 4)						
Resolution	N		12			Bits
Integral Nonlinearity	INL			±0.4	±3	LSB
Differential Nonlinearity	DNL	No missing codes over temperature		±0.25	±1	LSB
Offset Error					±0.5	%FS
Gain Error					±2.4	%FS
ANALOG INPUTS (IN_P, IN_N)						
Input Differential Range	V_{ID}	Differential input		1.4		V_{P-P}
Common-Mode Voltage Range	V_{CMO}			0.76		V
Common-Mode Voltage Range Tolerance		(Note 5)		±50		mV
Differential Input Impedance	R_{IN}	Switched capacitor load		2		kΩ
Differential Input Capacitance	C_{IN}			12.5		pF
CONVERSION RATE						
Maximum Conversion Rate	f_{SMAX}		40			MHz
Minimum Conversion Rate	f_{SMIN}			4.0		MHz
Data Latency				6.5		Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS (differential inputs, 4096-point FFT) (Note 4)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5.3MHz at -0.5dBFS		69.9		dB
		f_{IN} = 19.3MHz at -0.5dBFS	66.5	69.6		
Signal-to-Noise and Distortion (First 4 Harmonics)	SINAD	f_{IN} = 5.3MHz at -0.5dBFS		69.9		dB
		f_{IN} = 19.3MHz at -0.5dBFS	66.5	69.6		
Effective Number of Bits	ENOB	f_{IN} = 5.3MHz at -0.5dBFS		11.3		dB
		f_{IN} = 19.3MHz at -0.5dBFS		11.3		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5.3MHz at -0.5dBFS		96		dBc
		f_{IN} = 19.3MHz at -0.5dBFS	79	90		
Total Harmonic Distortion	THD	f_{IN} = 5.3MHz at -0.5dBFS		-96		dBc
		f_{IN} = 19.3MHz at -0.5dBFS		-92	-79	
Intermodulation Distortion	IMD	f_1 = 5.3MHz at -6.5dBFS f_2 = 6.3MHz at -6.5dBFS		89.8		dBc
Third-Order Intermodulation	IM3	f_1 = 5.3MHz at -6.5dBFS f_2 = 6.3MHz at -6.5dBFS		96.6		dBc
Aperture Jitter	t_{AJ}	Figure 11		< 0.4		ps_{RMS}
Aperture Delay	t_{AD}	Figure 11		1		ns
Small-Signal Bandwidth	SSBW	Input at -20dBFS		100		MHz
Full-Power Bandwidth	LSBW	Input at -0.5dBFS		100		MHz
Output Noise		IN_P = IN_N		0.44		LSB_{RMS}
Over-Range Recovery Time	t_{OR}	R_S = 25Ω, C_S = 50pF		1		Clock cycle
INTERNAL REFERENCE						
REFADJ Internal Reference-Mode Enable Voltage		(Note 6)			0.1	V
REFADJ Low-Leakage Current				1.5		mA
REFIO Output Voltage	V_{REFIO}		1.18	1.24	1.30	V
Reference Temperature Coefficient	TC_{REFIO}			120		ppm/°C
EXTERNAL REFERENCE						
REFADJ External Reference-Mode Enable Voltage		(Note 6)	V_{AVDD} - 0.1			V
REFADJ High-Leakage Current				200		µA
REFIO Input Voltage				1.24		V
REFIO Input Voltage Tolerance				±5		%
REFIO Input Current	I_{REFIO}			< 1		µA

Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMMON-MODE OUTPUT (CMOUT)						
CMOUT Output Voltage	V_{CMOUT}			0.76		V
CLOCK INPUT (CLK)						
Input High Voltage	V_{CLKH}		0.8 x V_{AVDD}			V
Input Low Voltage	V_{CLKL}				0.2 x V_{AVDD}	V
Clock Duty Cycle				50		%
Clock Duty-Cycle Tolerance				±30		%
Input Leakage Current	DI_{IN}	Input at GND			5	µA
		Input at AVDD			80	
Input Capacitance	DC_{IN}			5		pF
DIGITAL INPUTS (PLL_, LVDSTEST, DT, SLVS, STBY, $\overline{T}$/B)						
Input Logic-High Voltage	V_{IH}		0.8 x V_{AVDD}			V
Input Logic-Low Voltage	V_{IL}				0.2 x V_{AVDD}	V
Input Leakage Current	DI_{IN}	Input at GND			5	µA
		Input at AVDD			80	
Input Capacitance	DC_{IN}			5		pF
LVDS OUTPUTS (OUT_P, OUT_N), SLVS/$\overline{LVDS}$ = 0						
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω	250		450	mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω	1.125		1.375	V
Rise Time (20% to 80%)	t_{RL}	R_{TERM} = 100Ω, C_{LOAD} = 5pF		350		ps
Fall Time (80% to 20%)	t_{FL}	R_{TERM} = 100Ω, C_{LOAD} = 5pF		350		ps
SLVS OUTPUTS (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, FRAMEN), SLVS/$\overline{LVDS}$ = 1, DT = 1						
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω		205		mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω		220		mV
Rise Time (20% to 80%)	t_{RS}	R_{TERM} = 100Ω, C_{LOAD} = 5pF		320		ps
Fall Time (80% to 20%)	t_{FS}	R_{TERM} = 100Ω, C_{LOAD} = 5pF		320		ps
STANDBY MODE (STBY)						
STBY Fall to Output Enable	t_{ENABLE}			200		µs
STBY Rise to Output Disable	$t_{DISABLE}$			60		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
AVDD Supply Voltage Range	V_{AVDD}			1.7	1.8	1.9	V
OVDD Supply Voltage Range	V_{OVDD}			1.7	1.8	1.9	V
CVDD Supply Voltage Range	V_{CVDD}			1.7	1.8	3.6	V
AVDD Supply Current	I_{AVDD}	f_{IN} = 19.3MHz at -0.5dBFS	STBY = 0		337	380	mA
			STBY = 0, DT = 1		337		mA
			STBY = 1, standby, no clock input		37		mA
OVDD Supply Current	I_{OVDD}	f_{IN} = 19.3MHz at -0.5dBFS	STBY = 0		76	100	mA
			STBY = 0, DT = 1		99		mA
			STBY = 1, standby, no clock input		16		µA
CVDD Supply Current	I_{CVDD}	CVDD is used only to bias ESD-protection diodes on CLK input, Figure 2			0		mA
Power Dissipation	P_{DISS}	f_{IN} = 19.3MHz at -0.5dBFS			743	864	mW
TIMING CHARACTERISTICS (Note 8)							
Data Valid to CLKOUT Rise/Fall	t_{OD}	Figure 5 (Notes 7, 8)		(t_{SAMPLE}/24) - 0.15		(t_{SAMPLE}/24) + 0.15	ns
CLKOUT Output-Width High	t_{CH}	Figure 5			t_{SAMPLE}/12		ns
CLKOUT Output-Width Low	t_{CL}	Figure 5			t_{SAMPLE}/12		ns
FRAME Rise to CLKOUT Rise	t_{CF}	Figure 4 (Note 8)		(t_{SAMPLE}/24) - 0.15		(t_{SAMPLE}/24) + 0.15	ns
Sample CLK Rise to FRAME Rise	t_{SF}	Figure 4 (Note 8)		(t_{SAMPLE}/2) + 1.1		(t_{SAMPLE}/2) + 2.6	ns
Crosstalk		(Note 4)			-95		dB
Gain Matching	C_{GM}	f_{IN} = 5.3MHz (Note 4)			±0.1		dB
Phase Matching	C_{PM}	f_{IN} = 5.3MHz (Note 4)			±0.25		Degrees

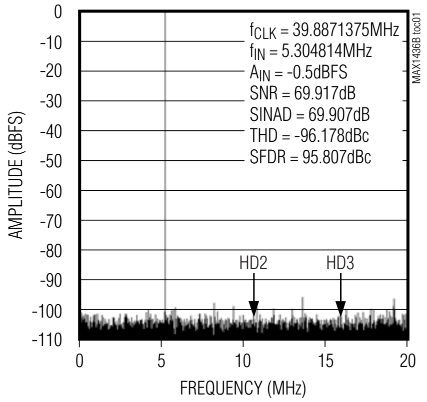
Note 2: Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization and not subject to production testing.
Note 3: All capacitances are between the indicated pin and GND, unless otherwise noted.
Note 4: See definition in the *Parameter Definitions* section at the end of this data sheet.
Note 5: See the *Common-Mode Output (CMOUT)* section.
Note 6: Connect REFADJ to GND directly to enable internal reference mode. Connect REFADJ to AVDD directly to disable the internal bandgap reference and enable external reference mode.
Note 7: Data valid to CLKOUT rise/fall timing is measured from 50% of data output level to 50% of clock output level.
Note 8: Guaranteed by design and characterization. Not subject to production testing.

Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

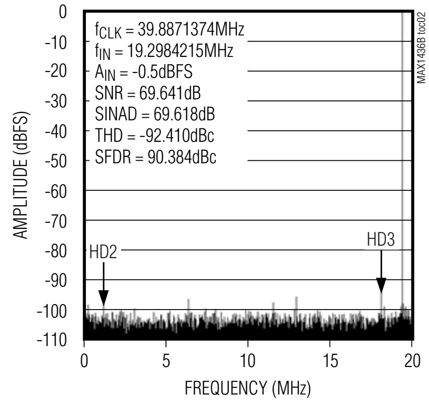
Typical Operating Characteristics

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

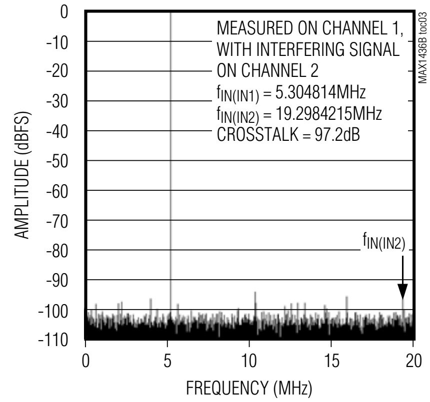
FFT PLOT (16,384-POINT DATA RECORD)



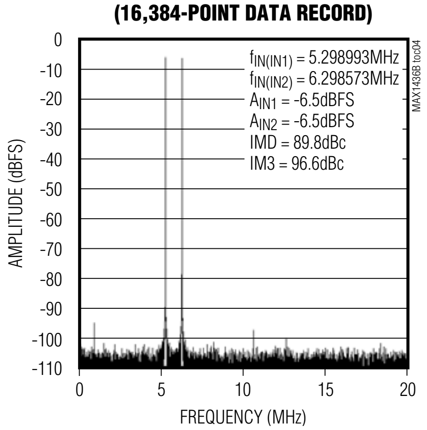
FFT PLOT (16,384-POINT DATA RECORD)



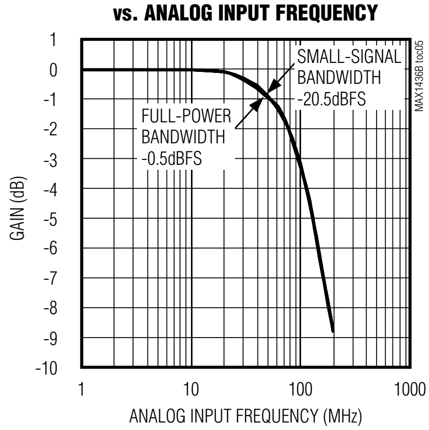
CROSSTALK (16,384-POINT DATA RECORD)



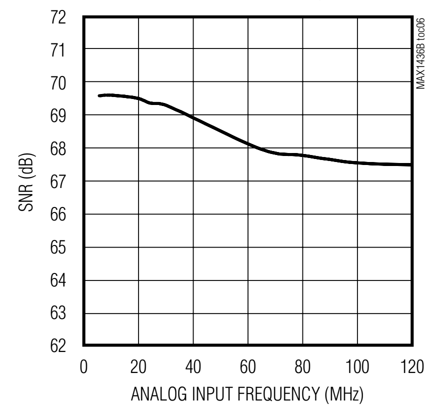
TWO-TONE INTERMODULATION DISTORTION (16,384-POINT DATA RECORD)



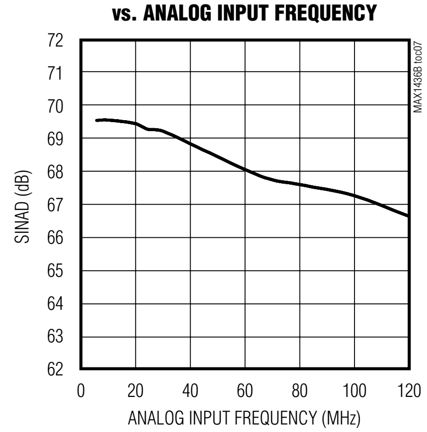
BANDWIDTH vs. ANALOG INPUT FREQUENCY



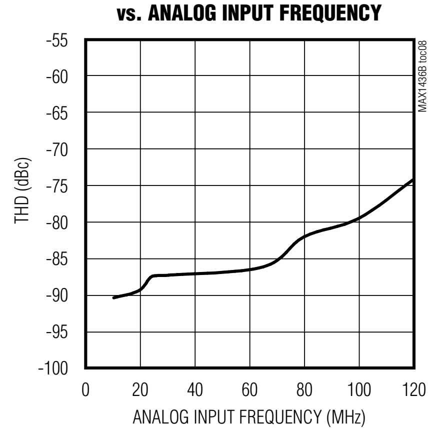
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



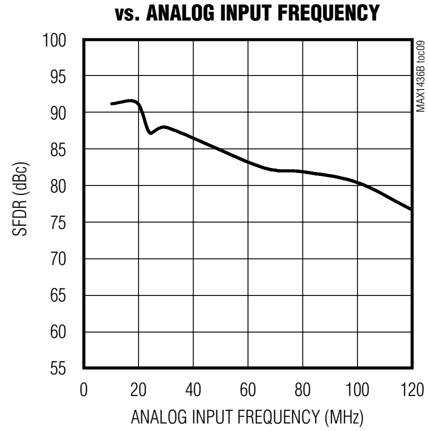
SIGNAL-TO-NOISE PLUS DISTORTION vs. ANALOG INPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



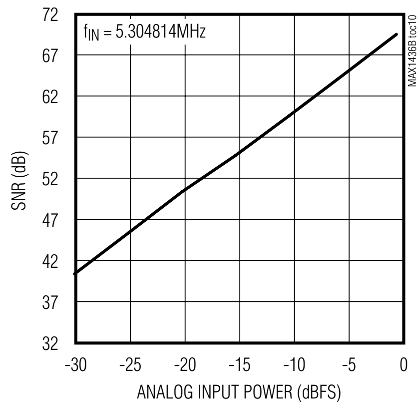
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



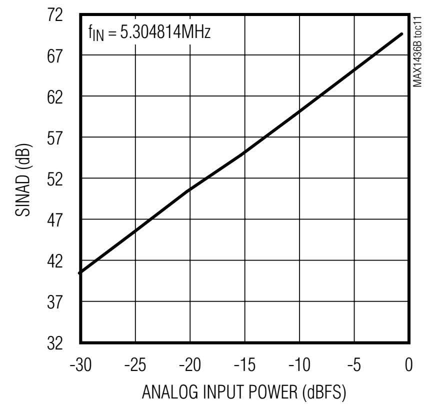
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

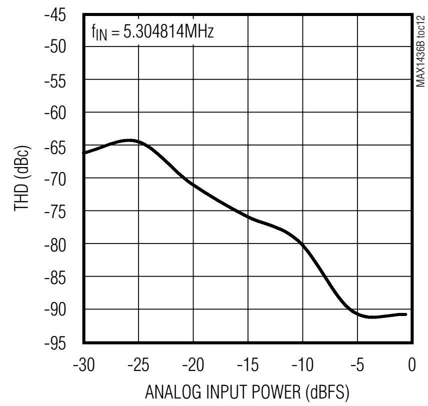
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT POWER



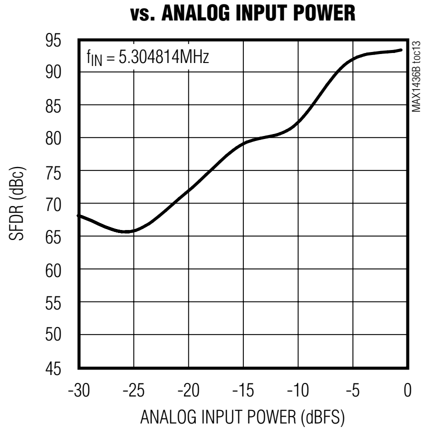
SIGNAL-TO-NOISE PLUS DISTORTION vs. ANALOG INPUT POWER



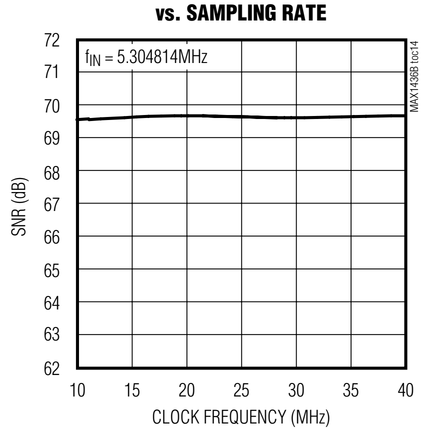
TOTAL HARMONIC DISTORTION vs. ANALOG INPUT POWER



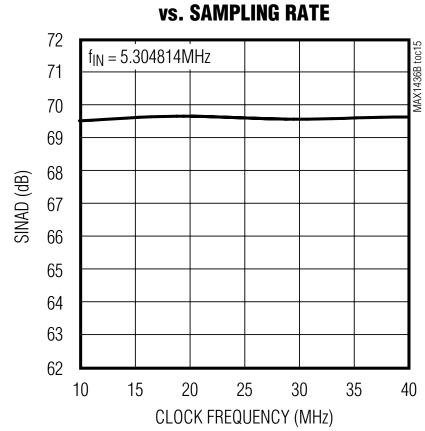
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER



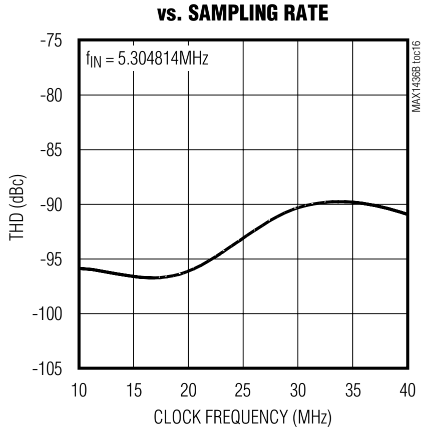
SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



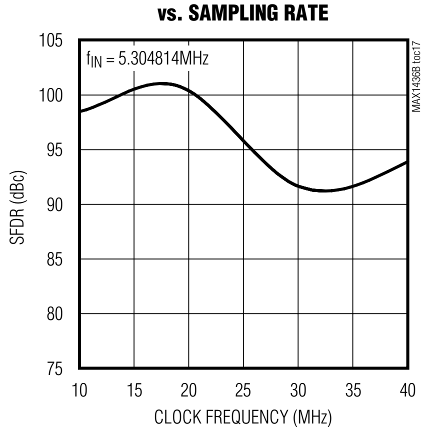
SIGNAL-TO-NOISE PLUS DISTORTION vs. SAMPLING RATE



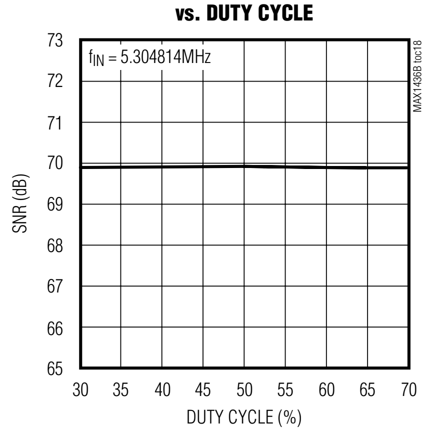
TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



SIGNAL-TO-NOISE RATIO vs. DUTY CYCLE

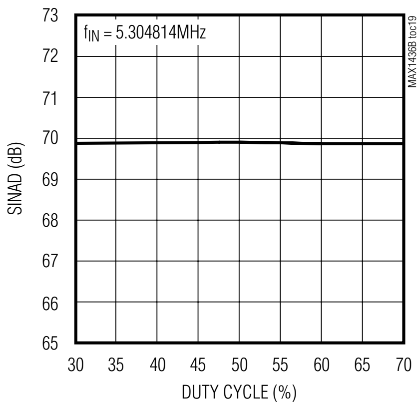


Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

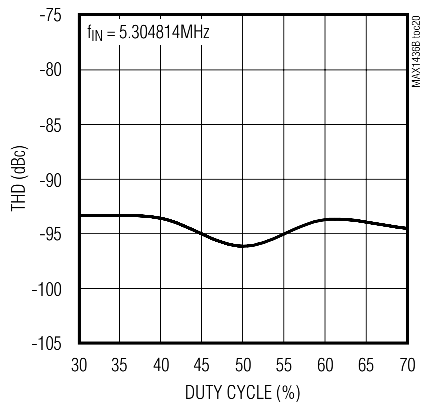
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

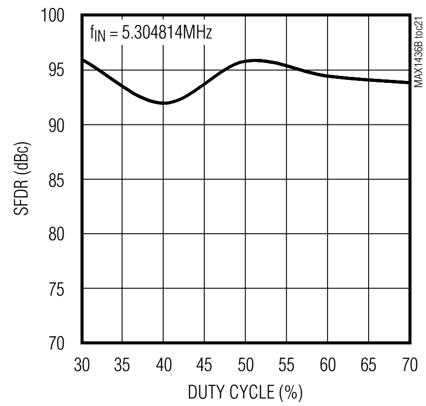
SIGNAL-TO-NOISE PLUS DISTORTION vs. DUTY CYCLE



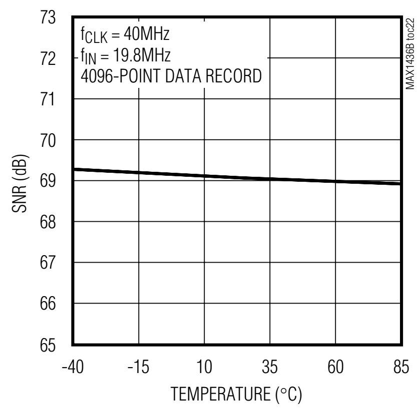
TOTAL HARMONIC DISTORTION vs. DUTY CYCLE



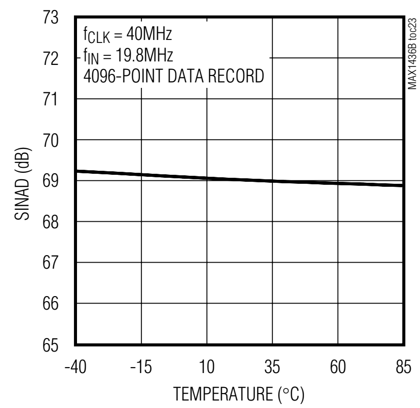
SPURIOUS-FREE DYNAMIC RANGE vs. DUTY CYCLE



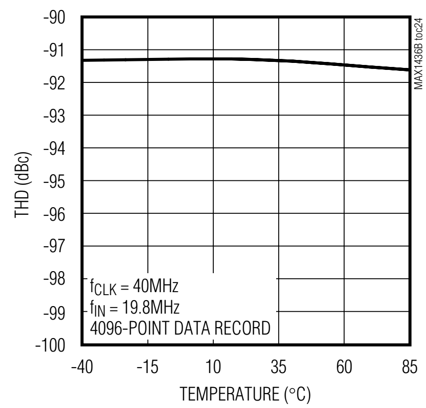
SIGNAL-TO-NOISE RATIO vs. TEMPERATURE



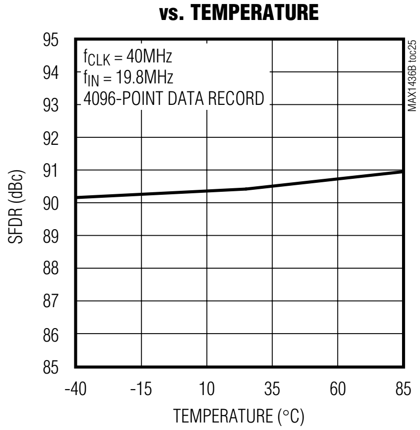
SIGNAL-TO-NOISE PLUS DISTORTION vs. TEMPERATURE



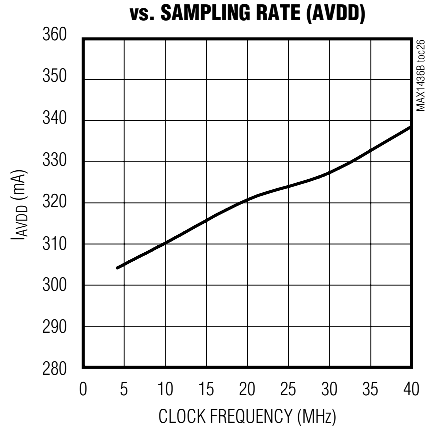
TOTAL HARMONIC DISTORTION vs. TEMPERATURE



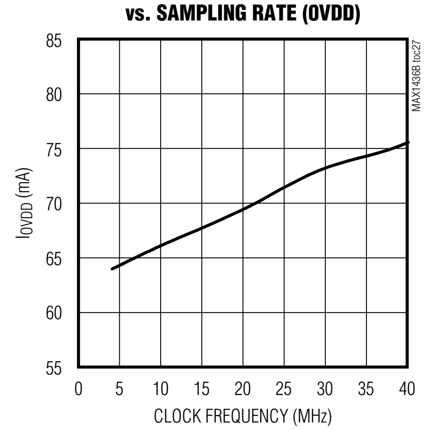
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



SUPPLY CURRENT vs. SAMPLING RATE (AVDD)



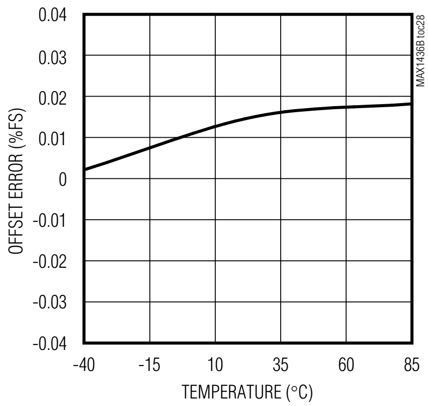
ANALOG SUPPLY CURRENT vs. SAMPLING RATE (OVDD)



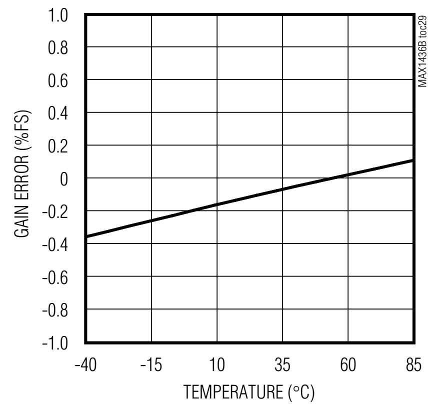
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

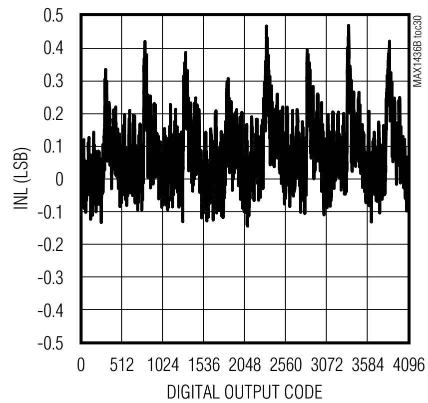
OFFSET ERROR vs. TEMPERATURE



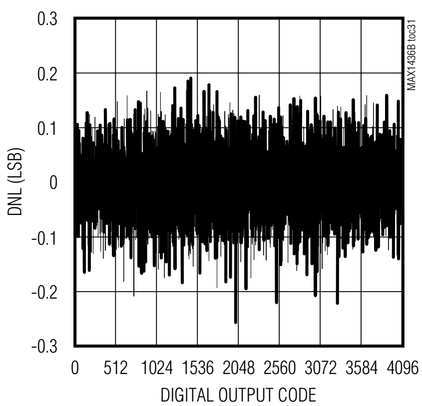
GAIN ERROR vs. TEMPERATURE



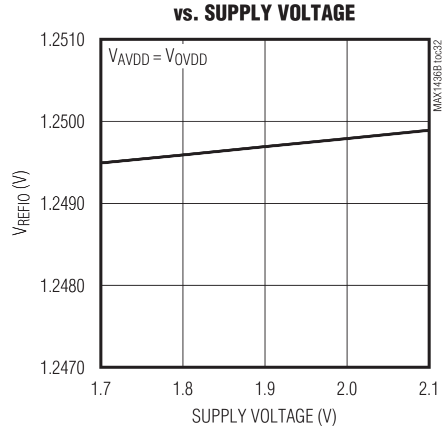
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



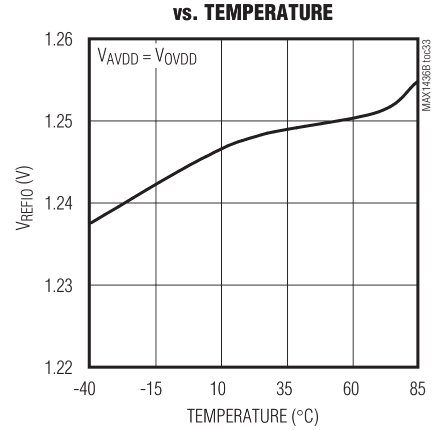
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE

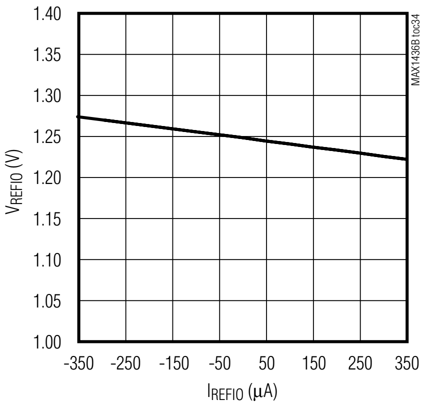


Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

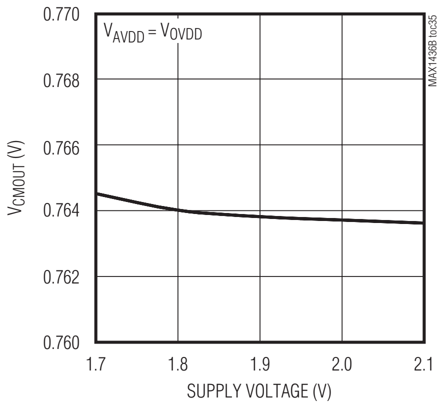
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 40MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

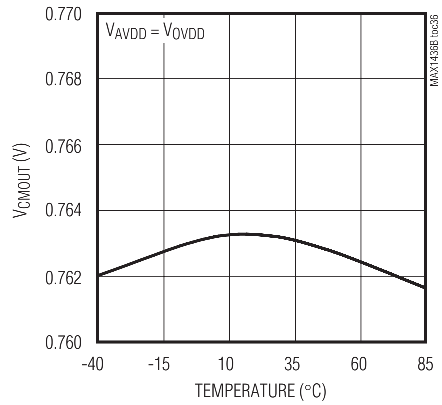
INTERNAL REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



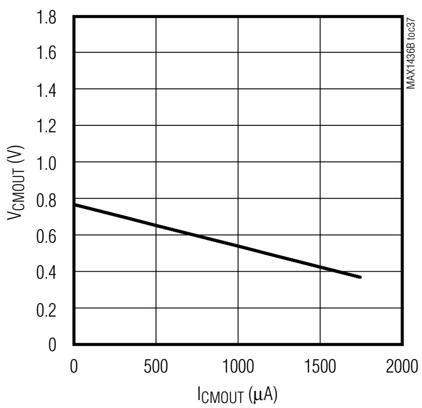
CMOUT VOLTAGE vs. SUPPLY VOLTAGE



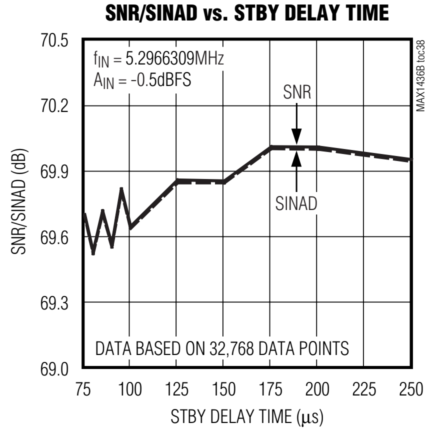
CMOUT VOLTAGE vs. TEMPERATURE



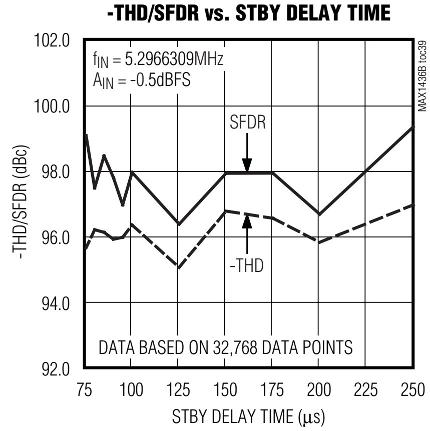
CMOUT VOLTAGE vs. LOAD CURRENT



SNR/SINAD vs. STBY DELAY TIME



-THD/SFDR vs. STBY DELAY TIME



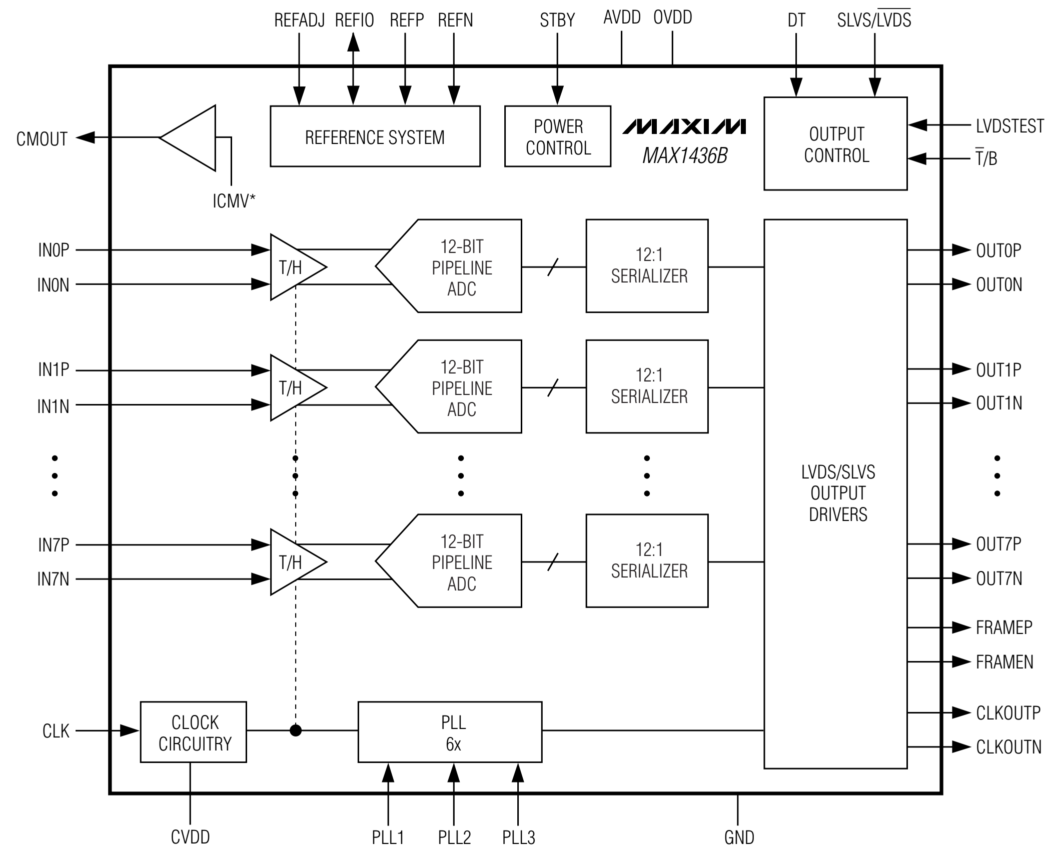
Pin Description

PIN	NAME	FUNCTION
1, 4, 7, 10, 16, 19, 22, 25, 26, 27, 30, 36, 89, 92, 96, 99, 100	GND	Ground. Connect all GND pins to the same potential.
2	IN1P	Channel 1 Positive Analog Input
3	IN1N	Channel 1 Negative Analog Input
5	IN2P	Channel 2 Positive Analog Input
6	IN2N	Channel 2 Negative Analog Input
8	IN3P	Channel 3 Positive Analog Input
9	IN3N	Channel 3 Negative Analog Input
11, 12, 13, 15, 37–42, 86, 87, 88	AVDD	Analog Power Input. Connect AVDD to a 1.7V to 1.9V power supply. Bypass AVDD to GND with a 0.1µF capacitor as close as possible to the device. Bypass the AVDD power plane to the GND plane with a bulk ≥ 2.2µF capacitor. Connect all AVDD pins to the same potential.
14, 31, 50, 51, 70, 75, 76	N.C.	No Connection. Not internally connected.
17	IN4P	Channel 4 Positive Analog Input
18	IN4N	Channel 4 Negative Analog Input
20	IN5P	Channel 5 Positive Analog Input
21	IN5N	Channel 5 Negative Analog Input
23	IN6P	Channel 6 Positive Analog Input
24	IN6N	Channel 6 Negative Analog Input
28	IN7P	Channel 7 Positive Analog Input
29	IN7N	Channel 7 Negative Analog Input
32	DT	Double-Termination Select. Drive DT high to select the internal 100Ω termination between the differential output pairs. Drive DT low to select no output termination.
33	SLVS/$\overline{\text{LVDS}}$	Differential Output-Signal Format-Select Input. Drive SLVS/$\overline{\text{LVDS}}$ high to select SLVS outputs. Drive SLVS/$\overline{\text{LVDS}}$ low to select LVDS outputs.
34	CVDD	Clock Power Input. Connect CVDD to a 1.7V to 3.6V power supply. Bypass CVDD to GND with a 0.1µF capacitor in parallel with a ≥ 2.2µF capacitor. Install the bypass capacitors as close as possible to the device.
35	CLK	Single-Ended CMOS Clock Input
43, 46, 49, 54, 57, 60, 63, 64, 67, 71, 74, 77	OVDD	Output-Driver Power Input. Connect OVDD to a 1.7V to 1.9V power supply. Bypass OVDD to GND with a 0.1µF capacitor as close as possible to the device. Bypass the OVDD power plane to the GND plane with a bulk ≥ 2.2µF capacitor. Connect all OVDD pins to the same potential.
44	OUT7N	Channel 7 Negative LVDS/SLVS Output
45	OUT7P	Channel 7 Positive LVDS/SLVS Output
47	OUT6N	Channel 6 Negative LVDS/SLVS Output
48	OUT6P	Channel 6 Positive LVDS/SLVS Output
52	OUT5N	Channel 5 Negative LVDS/SLVS Output
53	OUT5P	Channel 5 Positive LVDS/SLVS Output
55	OUT4N	Channel 4 Negative LVDS/SLVS Output
56	OUT4P	Channel 4 Positive LVDS/SLVS Output

Pin Description (continued)

PIN	NAME	FUNCTION
58	FRAMEN	Negative Frame-Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
59	FRAMEP	Positive Frame-Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
61	CLKOUTN	Negative LVDS/SLVS Serial Clock Output
62	CLKOUTP	Positive LVDS/SLVS Serial Clock Output
65	OUT3N	Channel 3 Negative LVDS/SLVS Output
66	OUT3P	Channel 3 Positive LVDS/SLVS Output
68	OUT2N	Channel 2 Negative LVDS/SLVS Output
69	OUT2P	Channel 2 Positive LVDS/SLVS Output
72	OUT1N	Channel 1 Negative LVDS/SLVS Output
73	OUT1P	Channel 1 Positive LVDS/SLVS Output
78	OUT0N	Channel 0 Negative LVDS/SLVS Output
79	OUT0P	Channel 0 Positive LVDS/SLVS Output
80	LVDSTEST	LVDS Test Pattern Enable. Drive LVDSTEST high to enable the output test pattern (0000 1011 1101 MSB → LSB). As with the analog conversion results, the test pattern data is output LSB first. Drive LVDSTEST low for normal operation.
81	STBY	Standby Input. An active-high level on STBY puts the MAX1436B into standby mode, leaving the reference circuitry active. Drive STBY low for normal operation.
82	PLL3	PLL Control Input 3. See Table 1 for details.
83	PLL2	PLL Control Input 2. See Table 1 for details.
84	PLL1	PLL Control Input 1. See Table 1 for details.
85	$\overline{T}$/B	Output Format-Select Input. Drive $\overline{T}$/B high to select binary output format. Drive $\overline{T}$/B low to select two's-complement output format.
90	REFN	Negative Reference Bypass Output. Connect a ≥ 1µF (10µF typ) capacitor between REFP and REFN, and connect a ≥ 1µF (10µF typ) capacitor between REFN and GND. **Place the capacitors as close as possible to the device on the same side of the PCB.**
91	REFP	Positive Reference Bypass Output. Connect a ≥ 1µF (10µF typ) capacitor between REFP and REFN, and connect a ≥ 1µF (10µF typ) capacitor between REFP and GND. **Place the capacitors as close as possible to the device on the same side of the PCB.**
93	REFIO	Reference Input/Output. For internal reference operation (REFADJ = GND), the reference output voltage is 1.24V. For external reference operation (REFADJ = AVDD), apply a stable reference voltage at REFIO. Bypass to GND with ≥ 0.1µF.
94	REFADJ	Internal/External Reference-Mode-Select and Reference Adjust Input. For internal reference mode, connect REFADJ directly to GND. For external reference mode, connect REFADJ directly to AVDD. For reference-adjust mode, see the *Full-Scale Range Adjustments Using the Internal Reference* section.
95	CMOUT	Common-Mode Reference Voltage Output. CMOUT outputs the input common-mode voltage for DC-coupled applications. Bypass CMOUT to GND with ≥ 0.1µF capacitor.
97	IN0P	Channel 0 Positive Analog Input
98	IN0N	Channel 0 Negative Analog Input
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to GND.

Functional Diagram



*ICMV = INPUT COMMON-MODE VOLTAGE (INTERNALLY GENERATED).

Detailed Description

The MAX1436B ADC features fully differential inputs, a pipelined architecture, and digital error correction for high-speed signal conversion. The ADC pipeline architecture moves the samples taken at the inputs through the pipeline stages every half clock cycle. The converted digital results are serialized and sent through the LVDS/SLVS output drivers. The total clock-cycle latency from input to output is 6.5 clock cycles.

The MAX1436B offers eight separate fully differential channels with synchronized inputs and outputs. Configure the outputs for binary or two's complement with the $\overline{\text{T}}$/B digital input. Global power-down minimizes power consumption.

Input Circuit

Figure 1 displays a simplified diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the operational transconductance amplifier (OTA), and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate

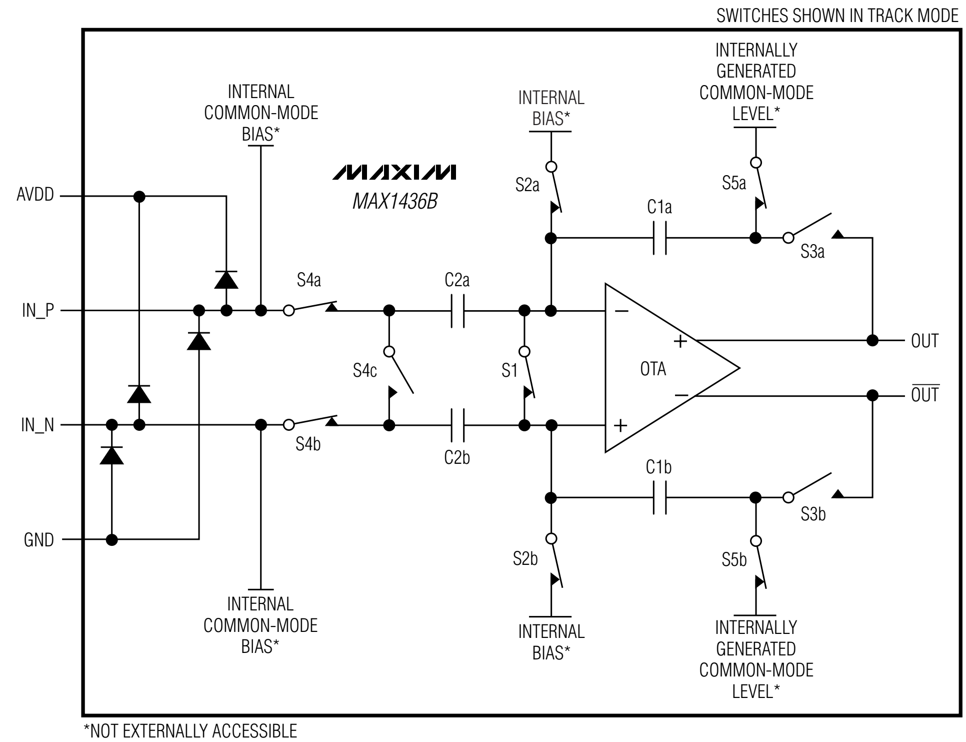


Figure 1. Internal Input Circuit

the pipelines from the fast-changing inputs. Analog inputs, IN_P to IN_N, are driven differentially. For differential inputs, balance the input impedance of IN_P and IN_N for optimum performance.

Reference Configurations (REFIO, REFADJ, REFP, and REFN)

The MAX1436B provides an internal 1.24V bandgap reference or can be driven with an external reference voltage. The full-scale analog differential input range is ±FSR. FSR (full-scale range) is given by the following equation:

$$FSR = \frac{(0.700 \times V_{REFIO})}{1.24V}$$

where V_{REFIO} is the voltage at REFIO, generated internally or externally. For a V_{REFIO} = 1.24V, the full-scale input range is ±700mV ($1.4V_{P-P}$).

Internal Reference Mode

Connect REFADJ to GND to use the internal bandgap reference directly. The internal bandgap reference generates V_{REFIO} to be 1.24V with a 120ppm/°C temperature coefficient in internal reference mode. Connect an external ≥ 0.1µF bypass capacitor from REFIO to GND for stability. REFIO sources up to 200µA and sinks up to 200µA for external circuits, and REFIO has a 75mV/mA load regulation. Putting the MAX1436B into standby mode turns off all circuitry except the reference circuit, allowing the converter to power-up faster when the ADC exits standby with a high-to-low transitional signal on STBY. The internal circuits of the MAX1436B require 200µs to power up and settle when the converter exits standby mode.

To compensate for gain errors or to decrease or increase the ADC's FSR, add an external resistor between REFADJ and GND or REFADJ and REFIO. This adjusts the internal reference value of the MAX1436B by up to ±5% of its nominal value. See the *Full-Scale Range Adjustments Using the Internal Reference* section.

Connect ≥ 1µF (10µF typ) capacitors to GND from REFP and REFN and a ≥ 1µF (10µF typ) capacitor between REFP and REFN as close to the device as possible on the same side of the PC board.

External Reference Mode

The external reference mode allows for more control over the MAX1436B reference voltage and allows multiple converters to use a common reference. Connect REFADJ to AVDD to disable the internal reference. Apply a stable 1.18V to 1.30V source at REFIO. Bypass REFIO to GND with a ≥ 0.1µF capacitor. The REFIO input impedance is > 1MΩ.

Clock Input (CLK)

The MAX1436B accepts a CMOS-compatible clock signal with a wide 20% to 80% input clock duty cycle. Drive CLK with an external single-ended clock signal. Figure 2 shows the simplified clock input diagram.

Low clock jitter is required for the specified SNR performance of the MAX1436B. Analog input sampling occurs on the rising edge of CLK, requiring this edge to provide the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter.

PLL Inputs (PLL1, PLL2, PLL3)

The MAX1436B features a PLL that generates an output clock signal with 6 times the frequency of the input clock. The output clock signal is used to clock data out of the MAX1436B (see the *System Timing Requirements* section). Set the PLL1, PLL2, and PLL3 bits according to the input clock range provided in Table 1.

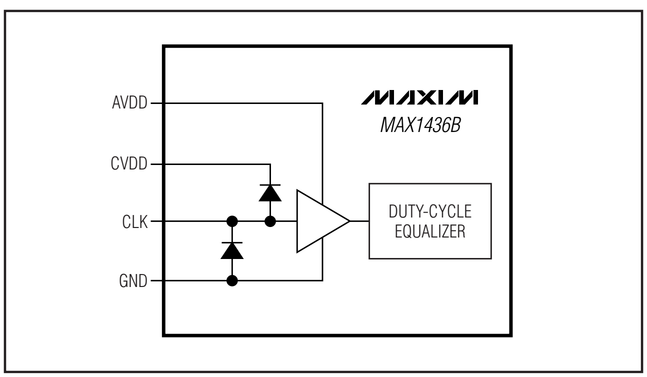


Figure 2. Clock Input Circuitry

Table 1. PLL1, PLL2, and PLL3 Configuration Table

PLL1	PLL2	PLL3	INPUT CLOCK RANGE (MHz)	
			MIN	MAX
0	0	0	Unused	
0	0	1	32.5	40.0
0	1	0	22.5	32.5
0	1	1	16.3	22.5
1	0	0	11.3	16.3
1	0	1	8.1	11.3
1	1	0	5.6	8.1
1	1	1	4.0	5.6

System Timing Requirements

Figure 3 shows the relationship between the analog inputs, input clock, frame-alignment output, serial-clock output, and serial-data output. The differential analog input (IN_P and IN_N) is sampled on the rising edge of the CLK signal and the resulting data appears at the digital outputs 6.5 clock cycles later. Figure 4 provides a detailed, two-conversion timing diagram of the relationship between the inputs and the outputs.

Clock Output (CLKOUTP, CLKOUTN)

The MAX1436B provides a differential clock output that consists of CLKOUTP and CLKOUTN. As shown in Figure 4, the serial output data is clocked out of the MAX1436B on both edges of the clock output. The frequency of the output clock is 6 times the frequency of CLK.

Frame-Alignment Output (FRAMEP, FRAMEN)

The MAX1436B provides a differential frame-alignment signal that consists of FRAMEP and FRAMEN. As shown in Figure 4, the rising edge of the frame-alignment signal corresponds to the first bit (D0) of the 12-bit serial data stream. The frequency of the frame-alignment signal is identical to the frequency of the input clock.

Serial Output Data (OUT_P, OUT_N)

The MAX1436B provides its conversion results through individual differential outputs consisting of OUT_P and OUT_N. The results are valid 6.5 input clock cycles after the sample is taken. As shown in Figure 3, the output data is clocked out on both edges of the output clock, LSB (D0) first. Figure 5 provides the detailed serial-output timing diagram.

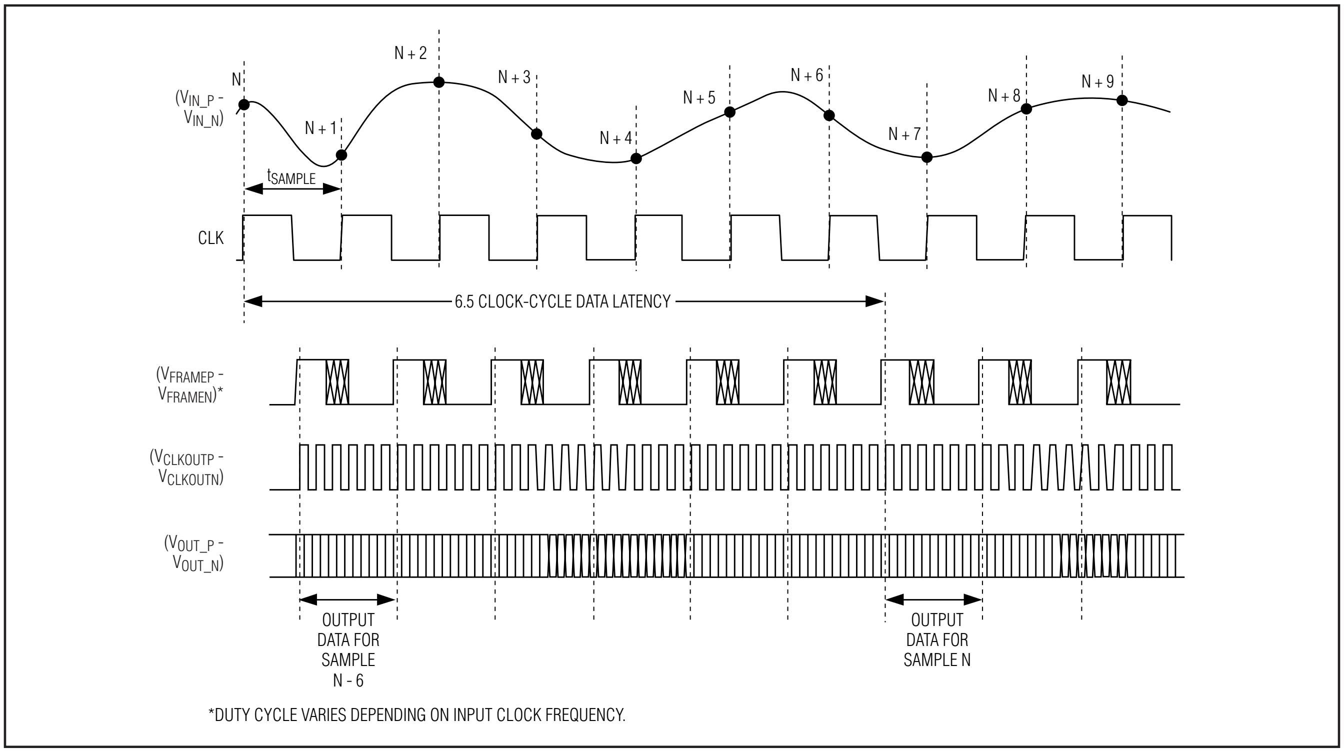


Figure 3. Global Timing Diagram

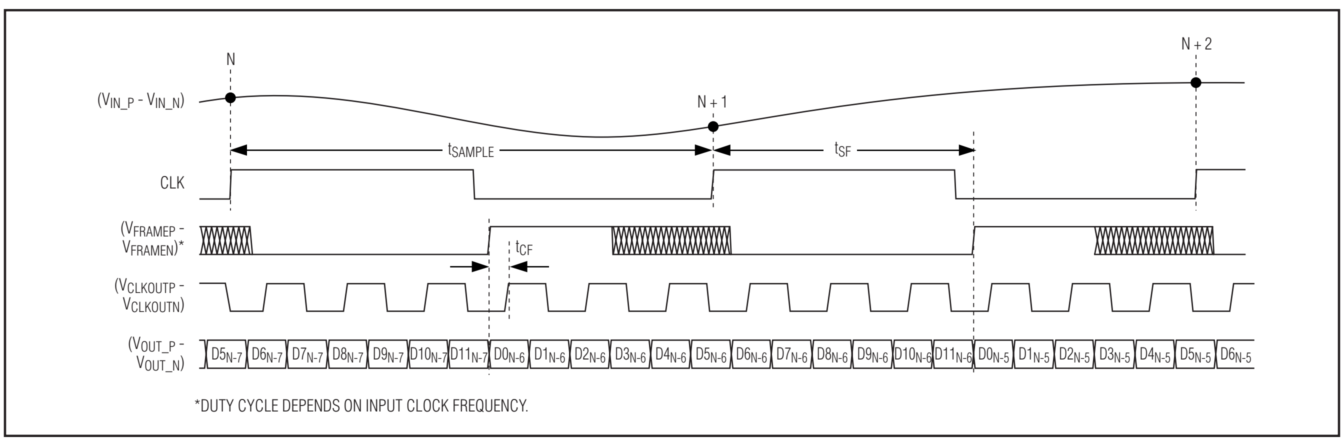


Figure 4. Detailed Two-Conversion Timing Diagram

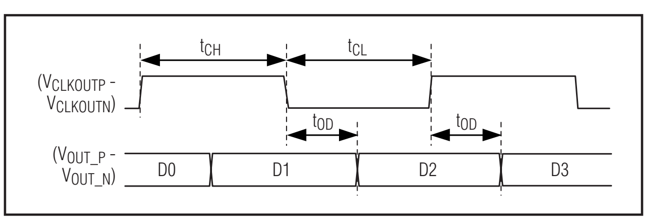


Figure 5. Serialized-Output Detailed Timing Diagram

Table 2. Output Code Table (V_{REFIO} = 1.24V)

TWO'S-COMPLEMENT DIGITAL OUTPUT CODE ($\overline{T}$/B = 0)			OFFSET BINARY DIGITAL OUTPUT CODE ($\overline{T}$/B = 1)			V_{IN_P} - V_{IN_N} (mV) (V_{REFIO} = 1.24V)
BINARY D11 → D0	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0	BINARY D11 → D0	HEXADECIMAL EQUIVALENT OF D11 → D0	DECIMAL EQUIVALENT OF D11 → D0	
0111 1111 1111	0x7FF	+2047	1111 1111 1111	0xFFF	+4095	+699.66
0111 1111 1110	0x7FE	+2046	1111 1111 1110	0xFFE	+4094	+699.32
0000 0000 0001	0x001	+1	1000 0000 0001	0x801	+2049	+0.34
0000 0000 0000	0x000	0	1000 0000 0000	0x800	+2048	0
1111 1111 1111	0xFFF	-1	0111 1111 1111	0x7FF	+2047	-0.34
1000 0000 0001	0x801	-2047	0000 0000 0001	0x001	+1	-699.66
1000 0000 0000	0x800	-2048	0000 0000 0000	0x000	0	-700.00

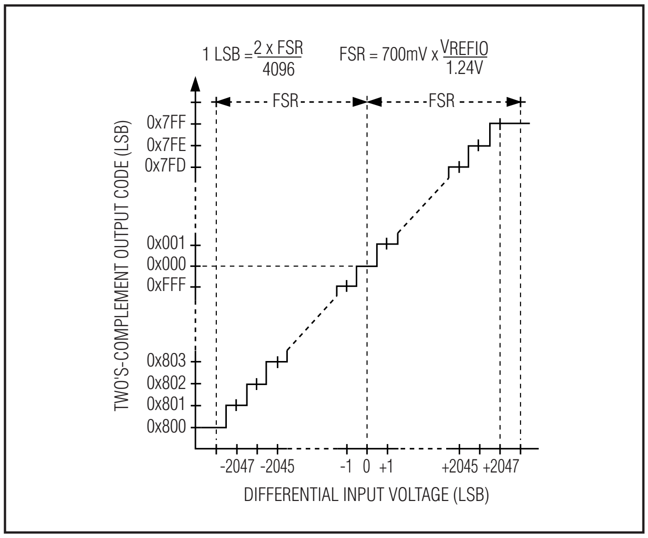


Figure 6. Two's-Complement Transfer Function ($\overline{T}$/B = 0)

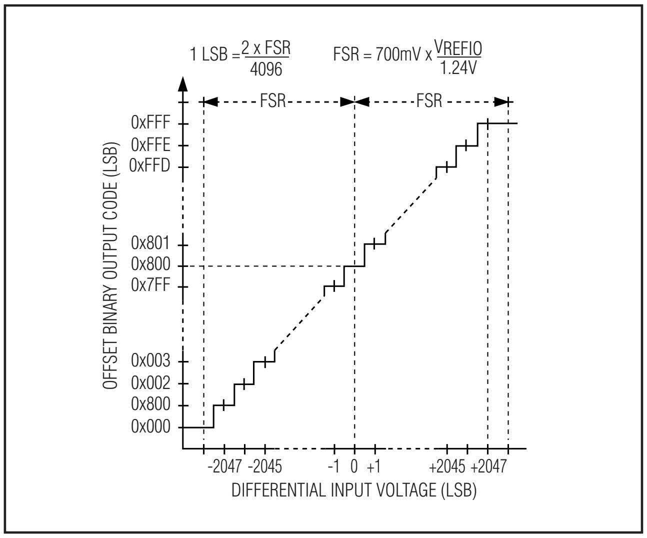


Figure 7. Binary Transfer Function ($\overline{T}$/B = 1)

Output Data Format ($\overline{T}$/B) Transfer Functions

The MAX1436B output data format is either offset binary or two's complement, depending on the logic-input $\overline{T}$/B. With $\overline{T}$/B low, the output data format is two's complement. With $\overline{T}$/B high, the output data format is offset binary. The following equations, Table 2, and Figures 6 and 7 define the relationship between the digital output and the analog input. For two's complement ($\overline{T}$/B = 0):

$$V_{IN\_P} - V_{IN\_N} = FSR \times 2 \times \frac{CODE_{10}}{4096}$$

and for offset binary ($\overline{T}$/B = 1):

$$V_{IN\_P} - V_{IN\_N} = FSR \times 2 \times \frac{CODE_{10} - 2048}{4096}$$

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 2.

Keep the capacitive load on the MAX1436B digital outputs as low as possible.

Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs

LVDS and SLVS Signals ($SLVS/\overline{LVDS}$)

Drive $SLVS/\overline{LVDS}$ low for LVDS or drive $SLVS/\overline{LVDS}$ high for SLVS levels at the MAX1436B outputs (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN). For SLVS levels, enable double-termination by driving DT high. See the *Electrical Characteristics* table for LVDS and SLVS output voltage levels.

LVDS Test Pattern (LVDSTEST)

Drive LVDSTEST high to enable the output test pattern on all LVDS or SLVS output channels. The output test pattern is 0000 1011 1101. Drive LVDSTEST low for normal operation (test pattern disabled).

Common-Mode Output (CMOUT)

CMOUT provides a common-mode reference for DC-coupled analog inputs. If the input is DC-coupled, match the output common-mode voltage of the circuit driving the MAX1436B to the output voltage at V_{CMOUT} to within ±50mV. It is recommended that the output common-mode voltage of the driving circuit be derived from CMOUT.

Double-Termination (DT)

The MAX1436B offers an optional, internal 100Ω termination between the differential output pairs (OUT_P and OUT_N, CLKOUTP and CLKOUTN, FRAMEP and FRAMEN). In addition to the termination at the end of the line, a second termination directly at the outputs helps eliminate unwanted reflections down the line. This feature is useful in applications where trace lengths are long (> 5in) or with mismatched impedance. Drive DT high to select double-termination, or drive DT low to disconnect the internal termination resistor (single-termination). Selecting double-termination increases the OVDD supply current (see Figure 8).

Standby Mode

The MAX1436B offers a standby mode to efficiently use power by transitioning to a low-power state when conversions are not required. STBY controls the standby mode of all channels and the internal reference circuitry. The reference does not power down in standby mode. Drive STBY high to enable standby. In standby mode, the output impedance of all of the LVDS/SLVS outputs is approximately 342Ω, if DT is low. The output impedance of the differential LVDS/SLVS outputs is 100Ω when DT is high. See the *Electrical Characteristics* table for typical supply currents during standby. The following list shows the state of the analog inputs and digital outputs in standby mode:

- IN_P, IN_N analog inputs are disconnected from the internal input amplifier
- Reference circuit remains active

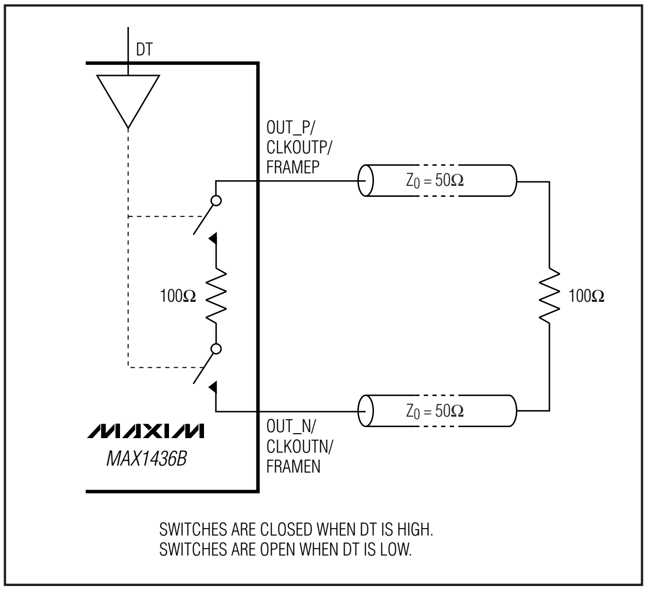


Figure 8. Double-Termination

- OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN have approximately 342Ω between the output pairs when DT is low. When DT is high, the differential output pairs have 100Ω between each pair.

When operating in internal reference mode, the MAX1436B requires 200µs to power up and settle when the converter exits standby mode. To exit standby mode, STBY, the applied control signal must transition from high to low. When using an external reference, the wake-up time is dependent on the external reference drivers.

Applications Information

Full-Scale Range Adjustments Using the Internal Reference

The MAX1436B supports a full-scale adjustment range of 10% (±5%). To decrease the full-scale range, add a 25kΩ to 250kΩ external resistor or potentiometer (R_{ADJ}) between REFADJ and GND. To increase the full-scale range, add a 25kΩ to 250kΩ resistor between REFADJ and REFIO. Figure 9 shows the two possible configurations.

The following equations provide the relationship between R_{ADJ} and the change in the analog full-scale range:

$$FSR = 0.7V\left(1 + \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and REFIO, and:

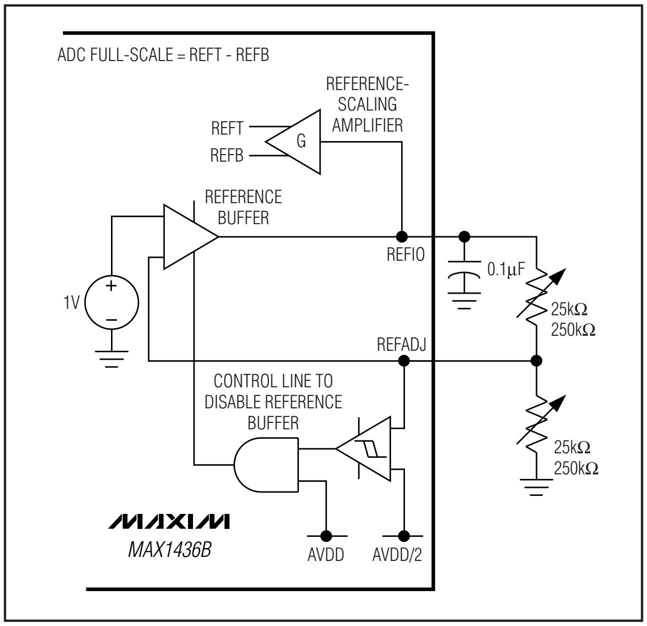


Figure 9. Circuit Suggestions to Adjust the ADC's Full-Scale Range

$$FSR = 0.7V\left(1 - \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and GND.

Using Transformer Coupling

An RF transformer (Figure 10) provides an excellent solution to convert a single-ended input source signal to a fully differential signal. The MAX1436B input common-mode voltage is internally biased to 0.76V (typ) with f_{CLK} = 40MHz. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion.

Grounding, Bypassing, and Board Layout

The MAX1436B requires high-speed board layout design techniques. Refer to the MAX1434/MAX1436/MAX1436B/MAX1437/MAX1438 EV kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass AVDD to GND with a 0.1µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor. Bypass OVDD to GND with a 0.1µF ceramic capacitor in parallel with a ≥ 2.2µF ceramic capacitor. Bypass CVDD to GND with a 0.1µF ceramic capacitor in parallel with a ≥ 2.2µF ceramic capacitor.

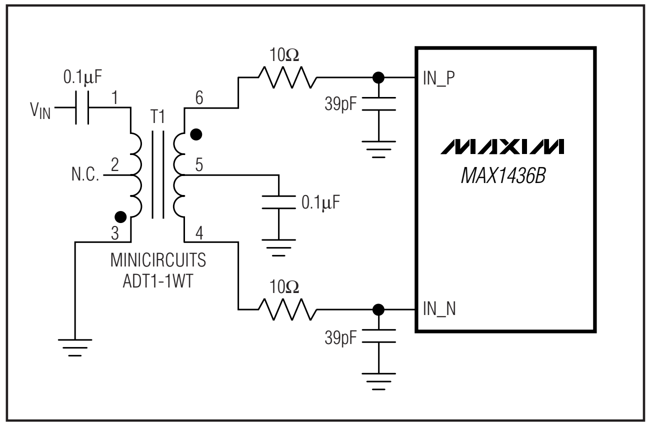


Figure 10. Transformer-Coupled Input Drive

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. Connect MAX1436B ground pins and the exposed pad to the same ground plane. The MAX1436B relies on the exposed-backside-pad connection for a low-inductance ground connection. Isolate the ground plane from any noisy digital system ground planes.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX1434/MAX1436/MAX1436B/MAX1437/MAX1438 EV kit data sheet for an example of symmetric input layout.

Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For the MAX1436B, this straight line is between the end points of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX1436B, DNL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

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Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. For the MAX1436B, the ideal midscale digital output transition occurs when there is -1/2 LSBs across the analog inputs (Figures 6 and 7). Bipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1436B the gain error is the difference of the measured full-scale and zero-scale transition points minus the difference of the ideal full-scale and zero-scale transition points.

For the bipolar devices (MAX1436B), the full-scale transition point is from 0x7FE to 0x7FF for two's-complement output format (0xFFE to 0xFFF for offset binary) and the zero-scale transition point is from 0x800 to 0x801 for two's complement (0x000 to 0x001 for offset binary).

Crosstalk

Crosstalk indicates how well each analog input is isolated from the others. For the MAX1436B, a 5.3MHz, -0.5dBFS analog signal is applied to one channel while a 19.3MHz, -0.5dBFS analog signal is applied to another channel. An FFT is taken on the channel with the 5.3MHz analog signal. From this FFT, the crosstalk is measured as the difference in the 5.3MHz and 19.3MHz amplitudes.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken. See Figure 11.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay. See Figure 11.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N \times 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc.

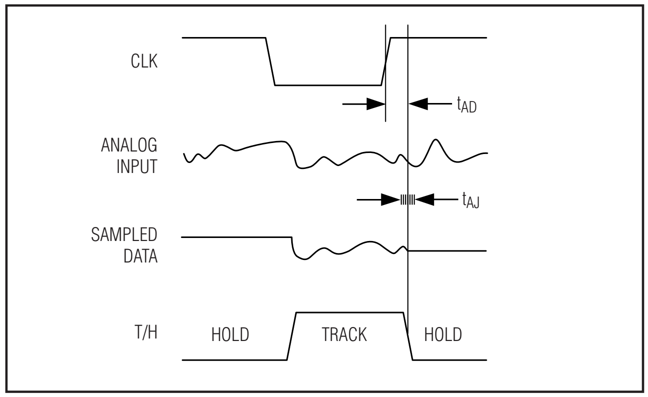

Figure 11. Aperture Jitter/Delay Specifications

For the MAX1436B, SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency, excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02} \right)$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1} \right)$$

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2. The individual input tone levels are at -6.5dBFS. The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): $f_1 + f_2$, $f_2 - f_1$
- 3rd-order intermodulation products (IM3): $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$
- 4th-order intermodulation products (IM4): $3 \times f_1 - f_2$, $3 \times f_2 - f_1$, $3 \times f_1 + f_2$, $3 \times f_2 + f_1$
- 5th-order intermodulation products (IM5): $3 \times f_1 - 2 \times f_2$, $3 \times f_2 - 2 \times f_1$, $3 \times f_1 + 2 \times f_2$, $3 \times f_2 + 2 \times f_1$

Third-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2. The individual input tone levels are at -6.5dBFS. The 3rd-order intermodulation products are $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$.

Small-Signal Bandwidth

A small -20.5dBFS analog input signal is applied to an ADC so that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

Gain Matching

Gain matching is a figure of merit that indicates how well the gain of all eight ADC channels is matched to each other. For the MAX1436B, gain matching is measured by applying the same 5.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 40Msps and the maximum deviation in amplitude is reported in dB as gain matching in the *Electrical Characteristics* table.

Phase Matching

Phase matching is a figure of merit that indicates how well the phases of all eight ADC channels are matched to each other. For the MAX1436B, phase matching is measured by applying the same 5.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 40Msps and the maximum deviation in phase is reported in degrees as phase matching in the *Electrical Characteristics* table.

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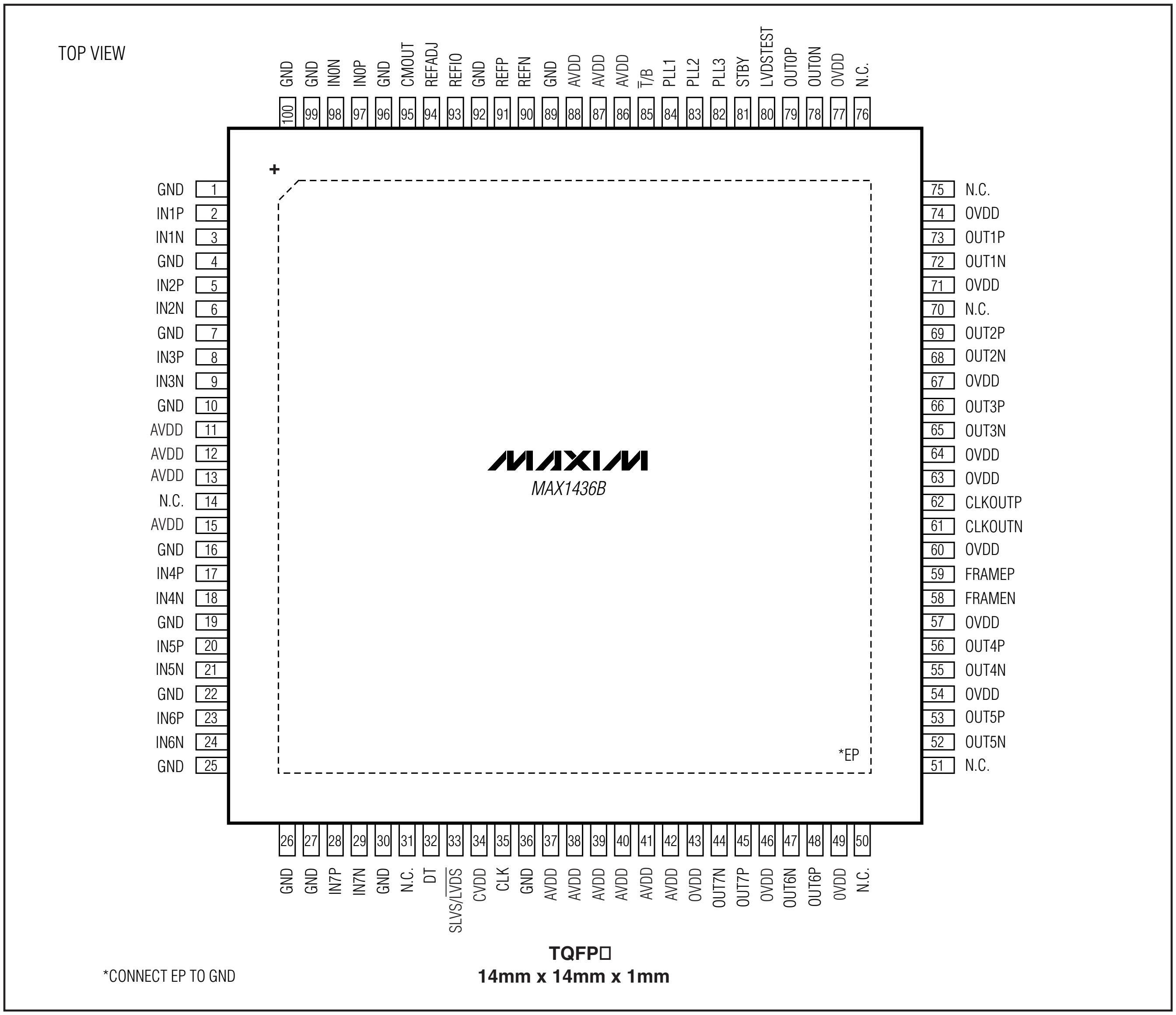
Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
100 TQFP-EP	C100E+2	**21-0116**	**90-0153**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/06	Initial release	—
1	2/11	Updated *Ordering Information*, added new *Package Thermal Characteristics* section, and fixed errors in *Electrical Characteristics* table	1–5