±15kV ESD protection, 3V **to** 5.5V **multi** -channel

RS-232 line driver and receiver

characteristic

It can be powered by a 3V to 5.5V VCC power supply.

ÿ Speed up to 250kbit/s

Two drivers and two receivers

Complies with the requirements of TIA/EIA-232-F and ITU V.28 standards.

Supports external small capacitors up to 0.1µF.

The serial pin provides enhanced ESD protection.

HBM Human Body Mode: ±15kV

IEC 61000-4-2: Contact discharge ±10kV;

Air discharge ±15kV.

DIP-16

SOP-16

TSSOP-16

Product Ordering Information

Product Name	Packaging	Print Name	Package	Packaging quantity
HGX3232AEIN	DIP-16	X3232AEI	Tube-	1000 pieces/box
HGX3232AEIM/TR	SOP-16	X3232AEI	type	2500 pieces/plate
HGX3232AEIMT/TR	TSSOP-16	3232AEI		2500 pieces/plate
HGX3232AECN	DIP-16	X3232AEC		1000 pieces/box
HGX3232AECM/TR	SOP-16	X3232AEC		2500 pieces/plate
HGX3232AECMT/TR	TSSOP-16	3232AEC	braided tape	2500 pieces/plate

Overview

The HGX3232A interface chip consists of two-channel drivers, two-channel receivers, and a dual-channel charge pump circuit, serial...
The port has ±15kV IEC ESD protection.

The HGX3232A complies with TIA/EIA-232-F requirements and provides [facilities] between the asynchronous communication controller and the serial port connector.
Electrical interface functionality. An internal charge pump and four external small capacitors support a single power supply from 3V to 5.5V.
The HGX3232A supports data signal transmission rates up to 250 kbit/s, and the driver output slew rate is up to 30 V/μs.

application

Industrial PC

Wired network

Data centers and enterprise computing

Battery-powered systems

Laptop

Handheld devices

Pin logic diagram and description

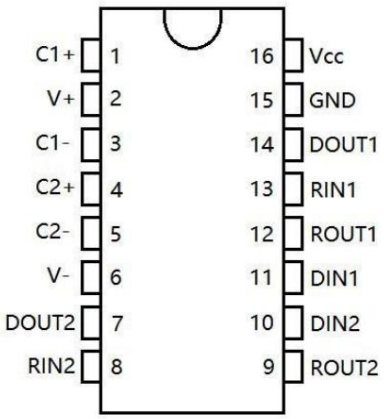


Figure 1: HGX3232A Pinout Diagram

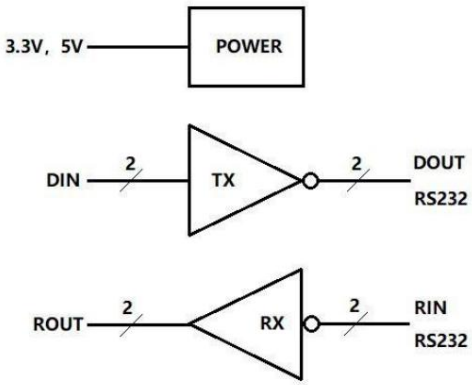


Figure 2: HGX3232A Logic Diagram

Pin Description

pin DIP/SOP/TSSOP	name	able
1	C1+ is the positive terminal of the voltage multiplier charge pump capacitor.	
2	V+ is the positive voltage generated by the charge pump.	
3	C1 – The negative terminal of the voltage multiplier charge pump capacitor.	
4	C2+ is the positive terminal of the anti-phase charge pump capacitor.	
5	C2 – The negative terminal of the reverse charge pump capacitor.	
6	V – The negative voltage generated by the charge pump.	
7	DOUT2 RS-232 driver output.	
8	RIN2	RS-232 receiver input.
9	ROUT2 TTL/CMOS receiver output.	
10	DIN2	TTL/CMOS driver input.
11	DIN1	TTL/CMOS driver input.
12	ROUT1 TTL/CMOS receiver output.	
13	RIN1	RS-232 receiver input.
14	DOUT1 RS-232 driver output.	
15	GND (Ground).	
16	VCC	+3.0V to +5.5V power supply.

Absolute maximum rating (1)

parameter	symbol	size	unit
Supply voltage;	VCC	+6	V
Charge pump output positive voltage (Note	V+	-0.3 to +7	V
2) ; Charge pump output negative voltage	V-	-0.3ÿ-7	V
(Note 2); Driver output voltage (Note 2)	V+ ~ V-	+13	V
Input voltage	Driver input	-0.3 to +6	V
	receiver input	-25ÿ25V	V
Output voltage	driver output	-13.2ÿ13.2V	V
	receiver output	-0.3ÿVCC+0.3	V
Storage temperature		-65ÿ+150	ÿ
Junction		+150	ÿ
temperature Welding temperature	TLEAD	+245	ÿ

Note: 1. Limiting parameters refer to the absolute values that must not be exceeded under any conditions. Exceeding these limits may cause physical damage such as product deterioration;
When the parameters are close to the limit, the chip cannot be guaranteed to work properly.
2. V+ and V- can reach a maximum voltage of 7V, but the difference between them cannot exceed 13V.

Recommended application conditions (Note 2)

Parameters:	Condition	Minimum value, typical value, maximum value, unit			
Power Supply Voltage	VCC = 3.3V	3	3.3	3.6	V
	VCC=5V	4.5	5	5.5	V
VIH driver input high voltage DIN	VCC=3.3V	2.0		5.5	V
	VCC=5V	2.4		5.5	V
VIL drive input low voltage DIN		0		0.8	V
VI receiver input voltage RIN operating		-25		25	V
temperature		-40		+85	ÿ

Note 2: When VCC=3.3V±0.3V, C1-C4=0.1μF; when VCC=5V±0.5V, C1=0.047μF, C2-C4=0.33μF.

Electrical characteristics (Note 3)

(Unless otherwise specified, when VCC=3.3V±0.3V, C1-C4=0.1μF; when VCC=5V±0.5V, C1=0.047μF, C2-C4=0.33μF; TA=25ÿ)

Parameter	symbol	Test conditions minimum typical maximum unit				
DC electrical characteristics						
Supply	ICC	unloaded, VCC=3.3V or 5.0V, TA=25ÿ		1.0		mA
current driver						
Driver output high	VOH	DOUT Load RL=3kÿ, DIN=GND 5		5.4		
voltage, driver output	VOL	DOUT Load RL=3kÿ, DIN=VCC	-5	-5.4		V
low voltage, driver input high level, input current	IIH	VI=VCC		±0.01	±1 μA	
to GND, driver input low level, input current;	IIL	VI connected		±0.01	±1 μA	
driver short-circuit, output current.	IOS	VCC=3.6V, VO=0V		±35	±60 mA	
		VCC=5.5V, VO=0V				
Driver output impedance	ro	VCC, V+ and V- = 0V, VO = ±2V	300	10M		ÿ
receiver						
Receiver output high voltage,	VOH	IOH=-1mA	VCC-0.6	VCC-0.2		V
receiver output low voltage,	VOL	IOL=1.6mA			0.4 mV	
positive input threshold voltage	VIT +	VCC = 3.3V		1.5	2.4	V
		VCC=5V		2.0	2.4	
Negative input threshold voltage	VIT -	VCC = 3.3V	0.6	1.1		V
		VCC=5V	0.8	1.5		
Hysteresis voltage	Vhys			0.4		V
input impedance	ri	VI = ±3V to ±25V	3	5	7	kÿ
ESD protection						
Electrostatic discharge protection (232 pins)	V(ESD)	HBM Human Body Model		±15		kV
		MM machine		±800		V
		mode contact discharge IEC		±10		kV
		61000-4-2 air discharge IEC 61000-4-2		±15		kV
Electrostatic discharge protection (other pins)	V(ESD)	HBM Human Body Model		±4		kV
		MM Machine Mode		±400		V

Note 3: Typical test conditions are VCC=3.3V or VCC=5V, TA=25ÿ.

Conversion characteristics

(Unless otherwise specified, when VCC=3.3V±0.3V, C1-C4=0.1μF; when VCC=5V±0.5V, C1=0.047μF, C2-C4=0.33μF; TA=25ÿ)

parameter	symbol	condition		Minimum	Typical	Maximum	Unit
Maximum data rate	F MAX	RL=3kÿ, CL=1000pF		250			kbps
Driver output skew |tPLH – tPHL|	tsk(p)	RL = 3kÿ to 7kÿ, CL = 150pF to 2500pF See Figure 3			100		ns
drive slew rate	SR(tr)	RL = 3kÿ to 7kÿ VCC=3.3V	CL = 150pF to 1000pF	6		30	V/μs
			CL = 150pF to 2500pF	4		30	
Receiver output delay from low to high tPLH		CL=150pF, see Figure 4			150		ns
Receiver output delay from high to low tPHL					150		ns
Receiver output skew |tPLH – tPHL|	tsk(p)				60		ns

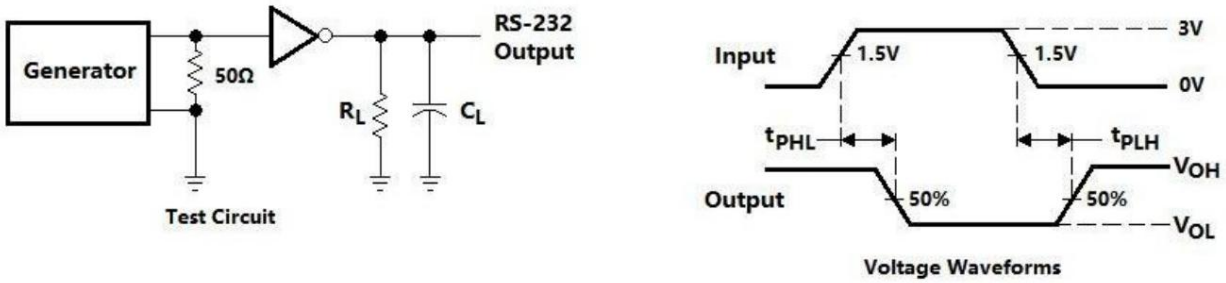


Figure 3: Driver waveform timing diagram

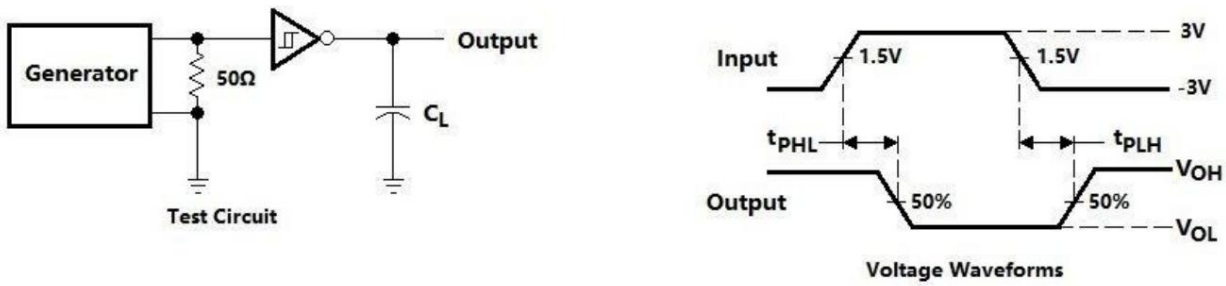


Figure 4: Receiver waveform timing diagram

Detailed description

Overview

The HGX3232A interface chip includes two drivers, two receivers, and a dual charge pump circuit. The serial port has...
±15kV IEC61000-4-2 ESD protection level. The HGX3232A complies with TIA/EIA-232-F requirements for asynchronous communication.
Electrical interface functionality is provided between the controller and the serial port connector. This is supported by an internal charge pump and four external small capacitors.
3V to 5.5V single power supply. The HGX3232A supports data signal transmission rates up to 250kbit/s, and the driver output...
The maximum slew rate is 30V/µs. The chip output port has short-circuit protection to ground.

powered by

The HGX3232A integrates a dual charge pump circuit to provide positive and negative voltages. The positive and negative voltages generated by the charge pumps are respectively...
On the chip's V+ and V- pins. This charge pump requires four external capacitors to operate normally.

RS232 driver

When the driver input DIN level is a valid high or low level, the driver will convert the TTL/CMOS standard logic level.
To comply with the RS232 level requirements of TIA/EIA-232-F.

RS232 Logic Function Table

The driver and receiver logic function tables for the HGX3232A are shown in Tables 1 and 2 below (H = high level, L = low level, Open = input open).

drive	
Enter **DIN**	Output **DOUT**
L	H
H	L

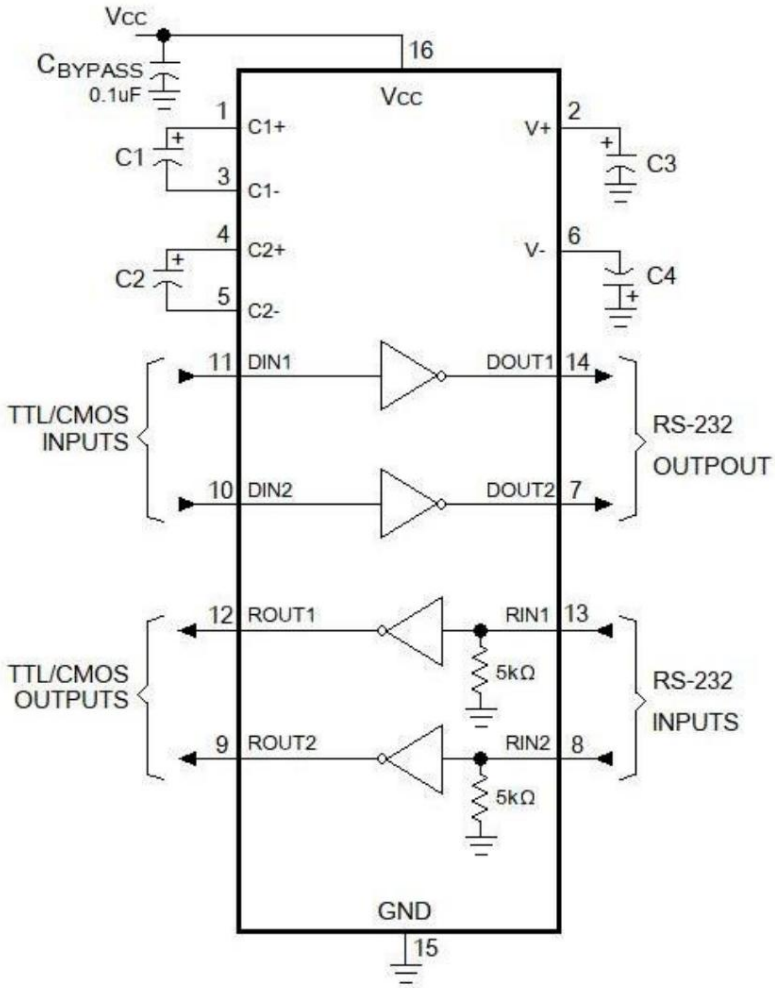
Table 1: Driver Logic Function Table

receiver	
Enter **RIN**	Output **ROUT**
L	H
H	L
Open	H

Table 2: Receiver Logic Function Table

Typical application (Note 4)

Figure 5 below shows a typical application diagram of the HGX3232A. The ROUT and DIN pins are connected to the UART port or general logic lines. On the way, RIN and DOUT



Connect the pins to the RS232 connector port or the RS232 bus. For proper operation, please refer to Table 3 to select the appropriate capacitor.

Figure 5: Typical application circuit diagram

Note 4: External capacitors can be non-polarized ceramic capacitors. If polarized tantalum capacitors or electrolytic capacitors are used, please refer to the polarity connection method in Figure 5 above.

vcc	C1	C2,C3,C4
3.3V±0.3V	0.1μF	0.1μF
5V±0.5V	0.047μF	0.33μF
3V to 5.5V	0.1μF	0.47μF

Table 3: Required Capacitor Values for VCC Voltage

PCB solutions

External capacitors should have the shortest possible traces, especially capacitors C1 and C2, as these two nodes have the fastest rise and fall times on the PCB.

Special attention is needed when laying out the map.

See Figure 6 below for a PCB reference example.

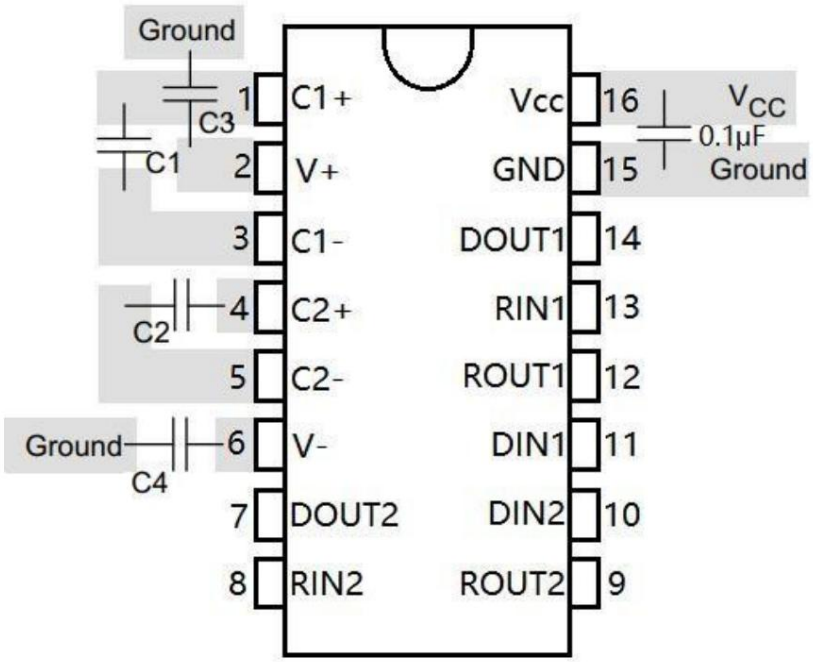
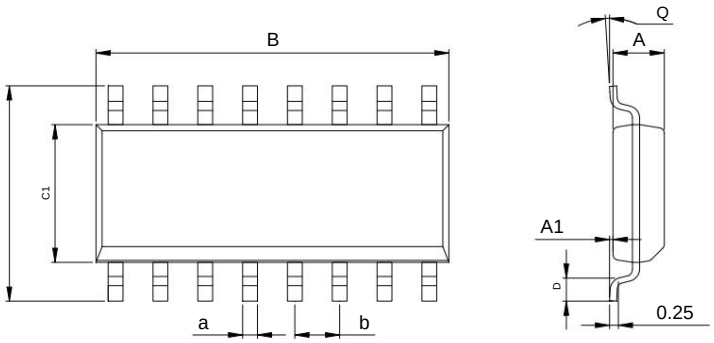


Figure 6: Example of PCB layout

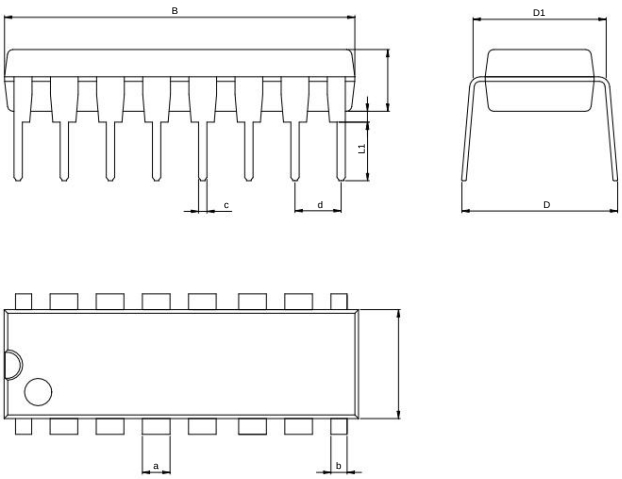
Package size

SOP-16



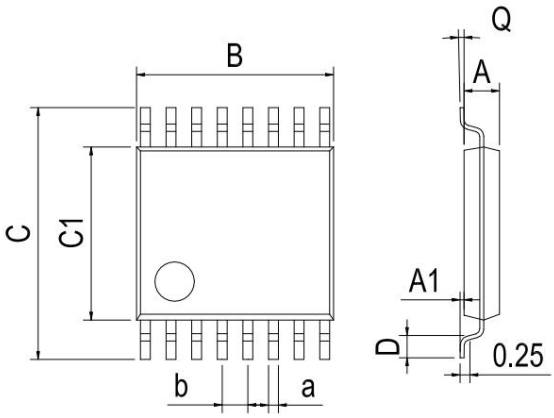
Dimensions In Millimeters(SOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

date	Modifications	page number
2017-11-5	Newly revised	1-12
2023-9-16	Modify TSSOP-16 package dimensions, update package, update pin soldering temperature, update DIP-16 dimensions, and add... Add limit parameter comments	1, 3, 9, 10

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